LeCroy Model 7242 1 GS/S Plug-In Module

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LeCROY MODEL 7242 1 GS/S PLUG-IN MODULE

SECTION 1 GENERAL INFORMATION

LeCroy's dual channel 7242 Plug-In Module, with its DC-400 MHz bandwidth, accurately captures fast waveforms. The Module can record single-shot signals with 1 nsec sampling resolution and 8-11 bits of vertical resolution. It can capture repetitive waveforms with 50 psec timing resolution and more than 11 bits of resolution.

The Module contains a deep 50 thousand point memory for storage of long waveform records. A full 50K of sample memory is provided to maintain a full 1 GS/sec digitizing rate with timebase settings as short as 5 usec/div.

FEATURES

- **Dual-channel 8-bit 1 GS/sec single shot recording**
- **50 ohm (DC) or 1 Mohm (AC or DC) input coupling**
- **DC to 400 MHz (-3dB) analog bandwidth for 50 ohm operation**
- **Continuously variable gain from 5 mV/div to 2.5 V/div, making full use of digitizing range**
- **50K sampling memory available on either channel**
- **12 - 48 divisions of offset control**
- **Internal time base. Provisions for connecting external time base**
- **Automatic synchronization of timebase and trigger with other 7200 series plug-in modules**
- **Real-time digital filtering that narrows bandwidth to increase resolution from 8 to 11 bits. Resolution can be enhanced further with signal averaging**
- **Random Interleaved Sampling (RIS) at 20 GS/sec with 50 ps resolution for repetitive waveforms**
- **Standard triggering plus SMART TRIGGER™ for easy triggering in difficult applications, including TV, pulse width, interval, logic, and others**
- **Continuously adjustable controls for timebase, trigger level, offset, etc.**
- **Keys (pushbuttons) for zeroing, trigger source selection, coupling, and slope**

- Rapid sequence mode acquisition capability (> 1 thousand sweeps/sec) with timestamping accurate to a single sample interval
- Fully programmable by remote control
- Automatic sensing of probe attenuator value
- Self-calibration
- Highly modular construction for easy serviceability

SECTION 2 TESTS

2-1 Introduction

Test procedures are provided for the purpose of verifying proper operation of the Plug-In Module and its ability to meet basic specifications. Tests are performed with the Plug-In Module installed in a known-good 7200 Precision Digital Oscilloscope (mainframe). This approach eliminates the 7200 Mainframe as a trouble source and isolates failures to boards or other components in the 7242 Plug-In Module such as the amplifier assemblies.

The normal procedure is to perform a turn-on test followed by nine NIST calibration tests. Use of traceable calibration standards ensures meeting NIST calibration criteria.

The nine NIST calibration tests are performed to exercise the 7242 Plug-In Module completely and isolate failures to specific circuitry. Individual tests can be performed to verify operation of specific circuitry as well. For this reason, setup instructions are repeated for each test.

In addition to NIST calibration testing, a system test can be performed to exercise individual subassemblies and additional tests described in the troubleshooting section (section 3) can be performed to isolate board level and component level problems.

2-2 Test Equipment

Performance of NIST calibration testing requires the following equipment:

A sinewave generator (Marconi 2019A, Tektronix SG504, or equivalent)

A square wave generator (LeCroy 9210/9211, Tektronix PG503, or equivalent)

A precision dc power supply (Date 8500, Tektronix PS5004, or equivalent)

2-3 Turn-On Test

The purpose of the turn-on test is to verify that the 7200 Mainframe can be turned on properly with the 7242 Plug-In Module installed.

2-3.1 Test Setup

To prepare the equipment for testing, do the following:

a. At Rear of 7200 mainframe, check line voltage setting of fuseholder (figure 2-1).

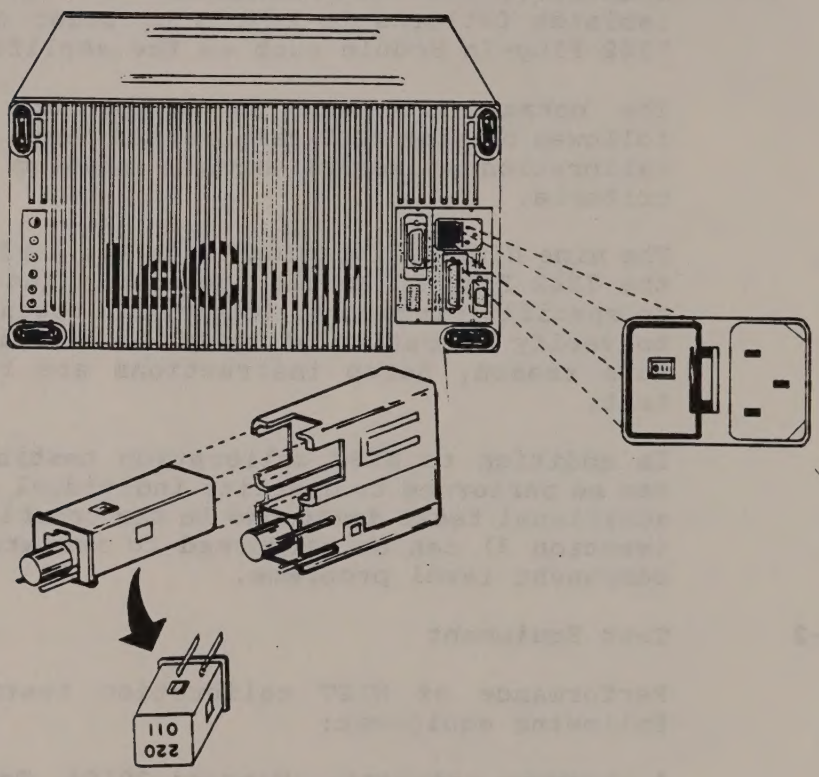


Figure 2-1. Line Voltage Setting

2-3.2 Test Procedure

NOTE

7200 Mainframe controls and indicators are identified and described in appendix A of the LeCroy 7200 Series Service Manual.

To perform the turn-on test, use the following procedure:

a. At front panel of 7200 Mainframe, press 1 on **POWER** switch to turn unit on.

2-3.3 Test Results

The main screen display (figure 2-2) will appear after approximately 5 seconds and the message **System Selftest Passed** will be displayed in the System Message Area, operating software is loaded from the hard disk drive, and the 7242 Plug-In Module is initialized.

After power is applied, operating software is loaded, and the 7242 Plug-In Module is initialized, the display on the 7200 Mainframe should be stable and the display of text and grids should visible and neither too dim nor too bright.

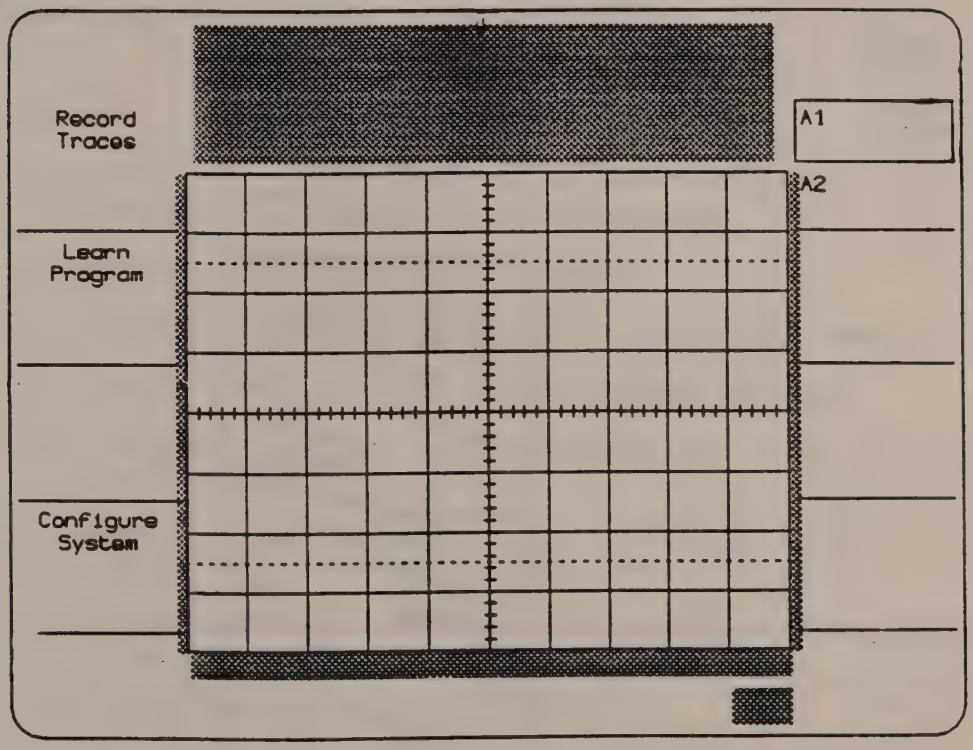


Figure 2-2. Main Screen

The 7242 Plug-in Module should be allowed a 20-minute warm-up period before other tests are performed. To adjust display brightness, refer to section 3, Adjustments, of the LeCroy 7200 Series Service Manual. If there is a turn-on test failure, replace the Module.

2-4 Baseline Noise Test

The purpose of the baseline noise test is to verify proper operation of front-end components. Baseline noise should not exceed 1 mV (sdev) on the 5 mV range of CH1 or CH2.

2-4.1 Test Setup

a. Connect 50 ohm terminators to CH1 and CH2 inputs of 7242 Plug-In Module (figure 2-3).

b. If test data are to be logged on a printer, connect an HP Thinkjet printer (or equivalent) to Centronics port on Rear of 7200 Mainframe.

c. Insert "CAL SETUP" diskette in floppy disk drive.

d. At front panel of 7200 Mainframe, press **CONFIGURE SYSTEM** softkey. You should see a screen display that resembles figure 2-4.

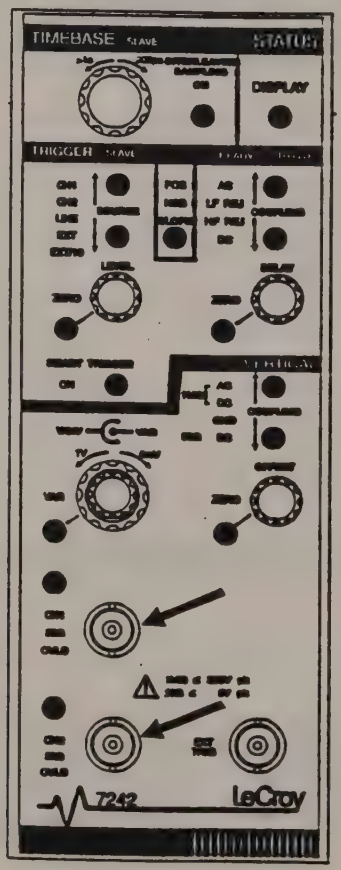


Figure 2-3. CH1 and CH2 Input Connectors

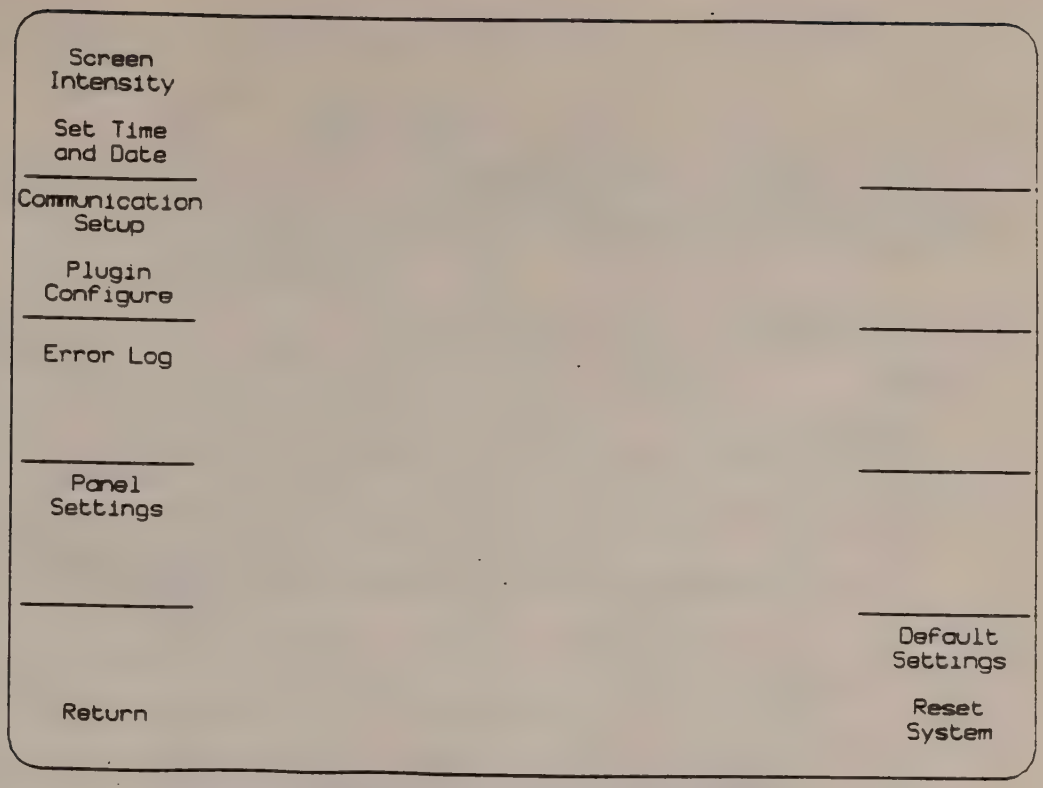


Figure 2-4. Configure System Screen

e. Press **DEFAULT SETTINGS** softkey.

f. Press **Yes DEFAULT** softkey. The 7200 will restart.

g. Press **MODIFY** key and **LEARN PROGRAM** softkey.

h. Rotate **Move Box** knob to highlight Disk in move select box.

i. Rotate **MODIFY VALUE** knob to select FLOPPY. The screen will resemble figure 2-5.

j. Rotate **Move Box** knob to move select box to RECALL FILE.

k. Select Recall Filename **NOISE**.

l. Press **Recall** softkey.

m. Press **Return** softkey (see figure 2-4).

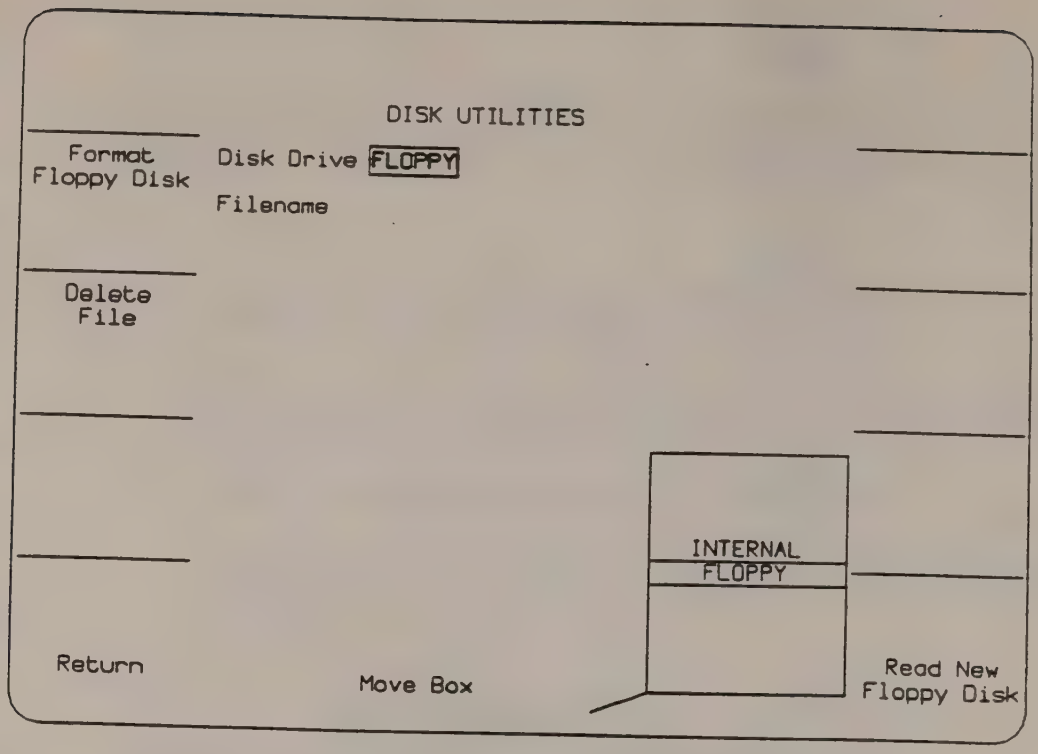


Figure 2-5. Floppy Disk Drive Selection Screen

2-4.3 Test Procedure

a. Press **Run Noise** softkey. The logging menu will be displayed.

b. Rotate **Move Cursor** knob to enter serial number of Module being tested.

c. Select output type:

1) LOG TO PRINTER (if HP Thinkjet printer or equivalent has been connected to Centronics port on rear of 7200 Mainframe and turned on)

2) LOG TO FLOPPY (If you wish to save test data on the internal 3.5-inch floppy disc drive) The filename will be the serial number of the Module under test, e.g., A85500.HCP.

3) NO LOG (if test results are to be displayed only on screen and not logged)

d. Press Return softkey. Program will switch through all time/div settings between 5 ms and 5 ns and log sdev noise for each channel at each setting for 5 seconds. Data table similar to figure 2-6 will be displayed if you selected NO LOG as the output type. Otherwise, data table will be stored on floppy disc or printed out.

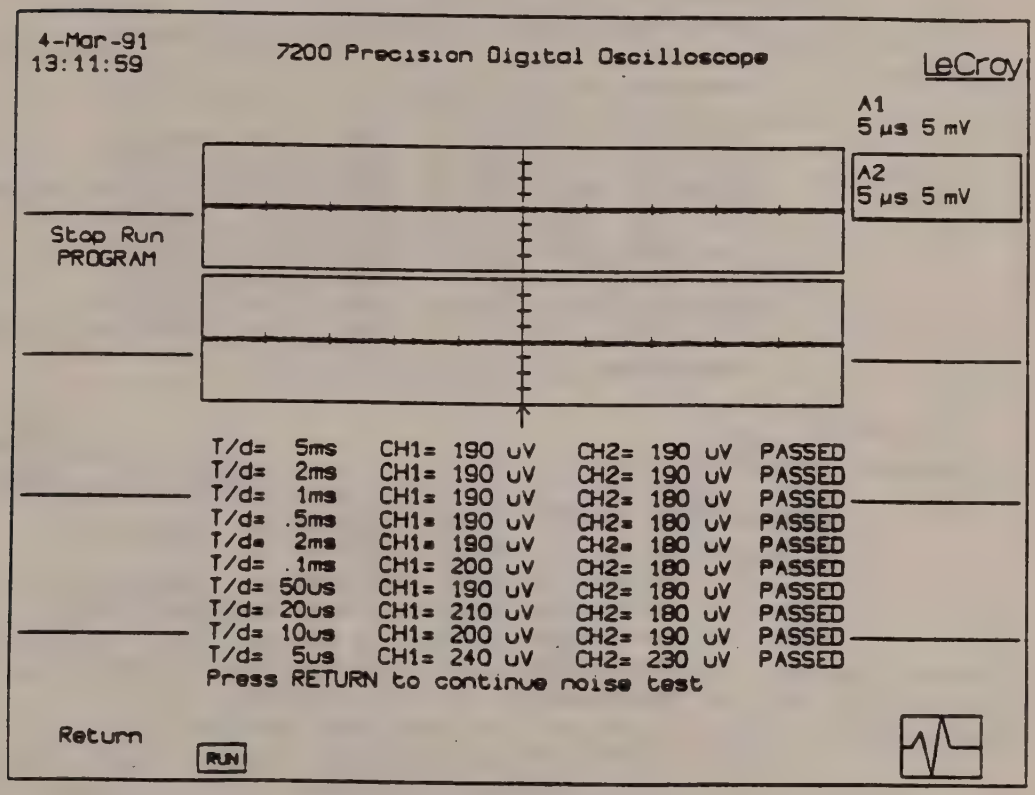

4-Mar-91
13:11:59
7200 Precision Digital Oscilloscope
LeCroy
A1
5 µs 5 mV
A2
5 µs 5 mV
Stop Run
PROGRAM
T/d= 5ms CH1= 190 uV CH2= 190 uV PASSED
T/d= 2ms CH1= 190 uV CH2= 190 uV PASSED
T/d= 1ms CH1= 190 uV CH2= 180 uV PASSED
T/d= .5ms CH1= 190 uV CH2= 180 uV PASSED
T/d= 2ms CH1= 190 uV CH2= 180 uV PASSED
T/d= .1ms CH1= 200 uV CH2= 180 uV PASSED
T/d= 50us CH1= 190 uV CH2= 180 uV PASSED
T/d= 20us CH1= 210 uV CH2= 180 uV PASSED
T/d= 10us CH1= 200 uV CH2= 190 uV PASSED
T/d= 5us CH1= 240 uV CH2= 230 uV PASSED
Press RETURN to continue noise test
Return
RUN

Figure 2-6. Test Data Display (Typical)

e. Press Return softkey to continue test. Program will switch through all time/div settings between 2 ms and 5 us. Test data will be displayed, stored on floppy disk, or printed. If the noise limit has been exceeded at any time base setting, test data entry or entries will be identified by asterisks as in figure 2-7.

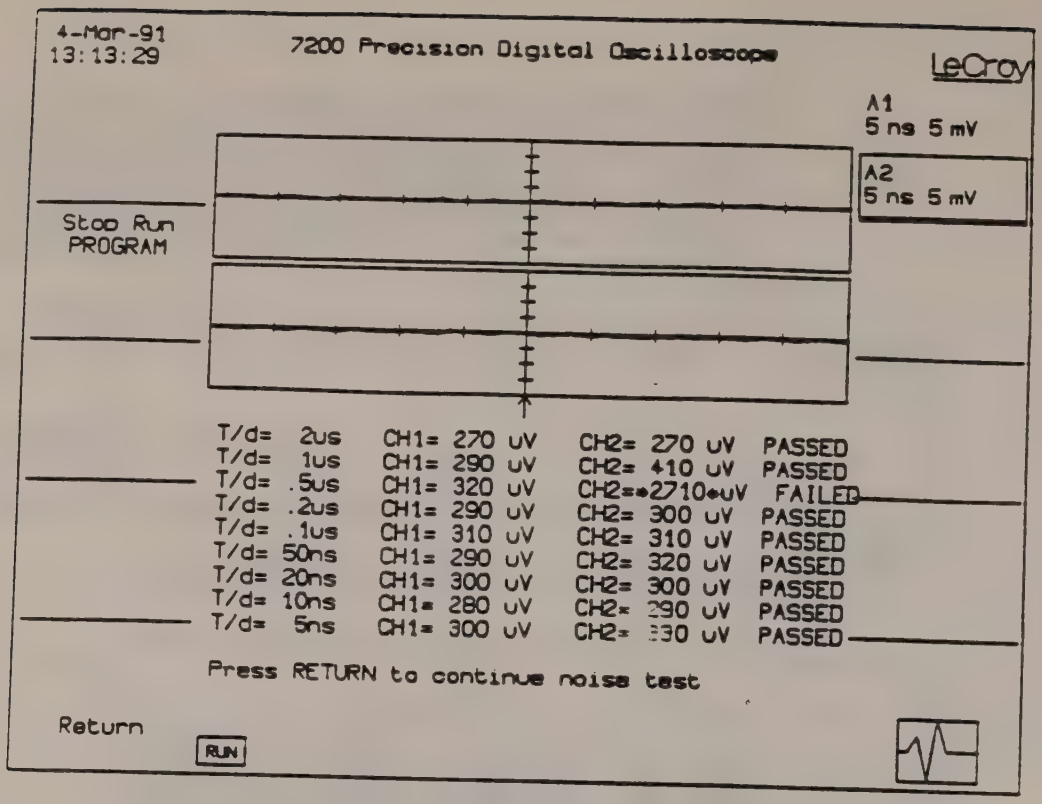

4-Mar-91
13:13:29
7200 Precision Digital Oscilloscope
LeCroy
A1
5 ns 5 mV
A2
5 ns 5 mV
Stop Run
PROGRAM
T/d= 2us CH1= 270 uV CH2= 270 uV PASSED
T/d= 1us CH1= 290 uV CH2= 410 uV PASSED
T/d= .5us CH1= 320 uV CH2=*2710*uV FAILED
T/d= .2us CH1= 290 uV CH2= 300 uV PASSED
T/d= .1us CH1= 310 uV CH2= 310 uV PASSED
T/d= 50ns CH1= 290 uV CH2= 320 uV PASSED
T/d= 20ns CH1= 300 uV CH2= 300 uV PASSED
T/d= 10ns CH1= 280 uV CH2= 290 uV PASSED
T/d= 5ns CH1= 300 uV CH2= 330 uV PASSED
Press RETURN to continue noise test
Return
RUN

Figure 2-7. Failed Range Notation (Typical)

f. Press Return softkey to continue test. The program will switch through all time/div settings between 2 us and 5 ns. Test data will be displayed, stored on floppy disk, or printed.

g. Press Return softkey again. Test data record will indicate **PASSED** as in figure 2-8 or **FAILED**.

2-4.4 Test Results

Input noise (sdev) should be less than 1 mV for all ranges. Any noise level in excess of 1 mV indicates the need for troubleshooting and repair.

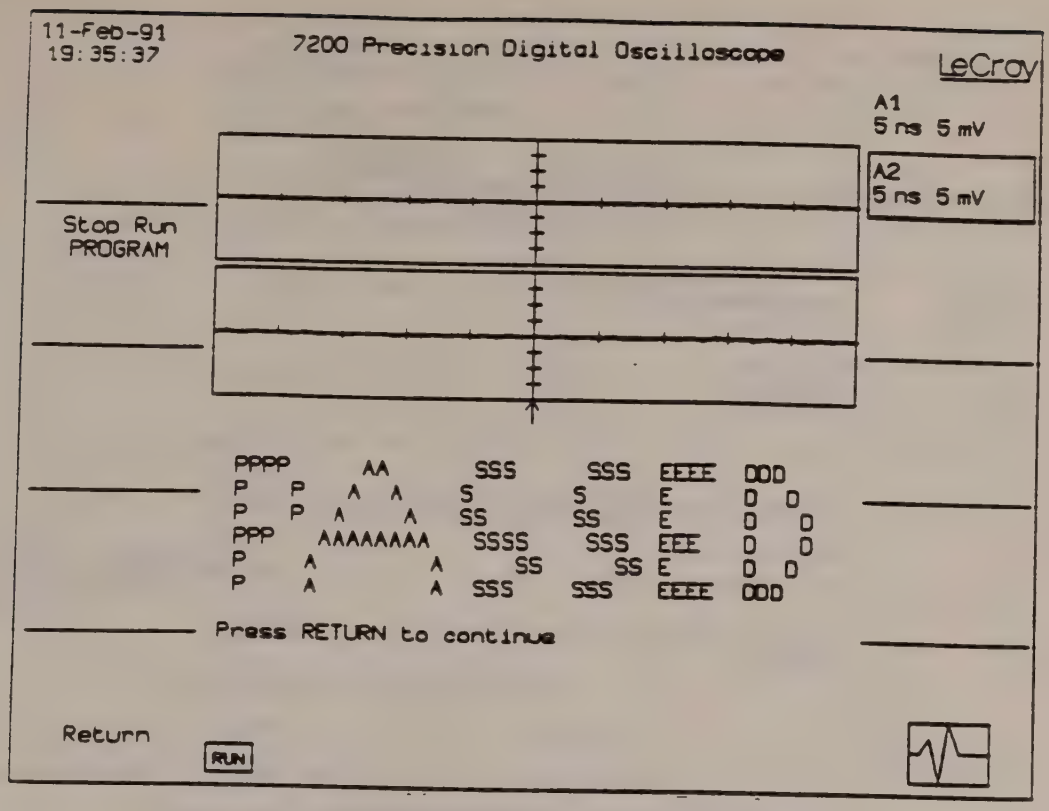


Figure 2-8. Test Passed Display (Typical)

2-5 Analog/Digital Converter Test

The purpose of this test is to verify proper operation of the analog/digital converters on the ADC(A) board for time base settings of 10us/div, 5us/div, and 2us/div.

2-5.1 Test Setup

To set up this test, use the following procedure:

a. Connect 50 ohm terminators to the CH1 and CH2 inputs (see figure 2-3).

b. On main screen display (see figure 2-2), press **Configure System** softkey. You should see a display that resembles figure 2-4.

c. Press **Panel Settings** softkey. You should see a display that resembles figure 2-9.

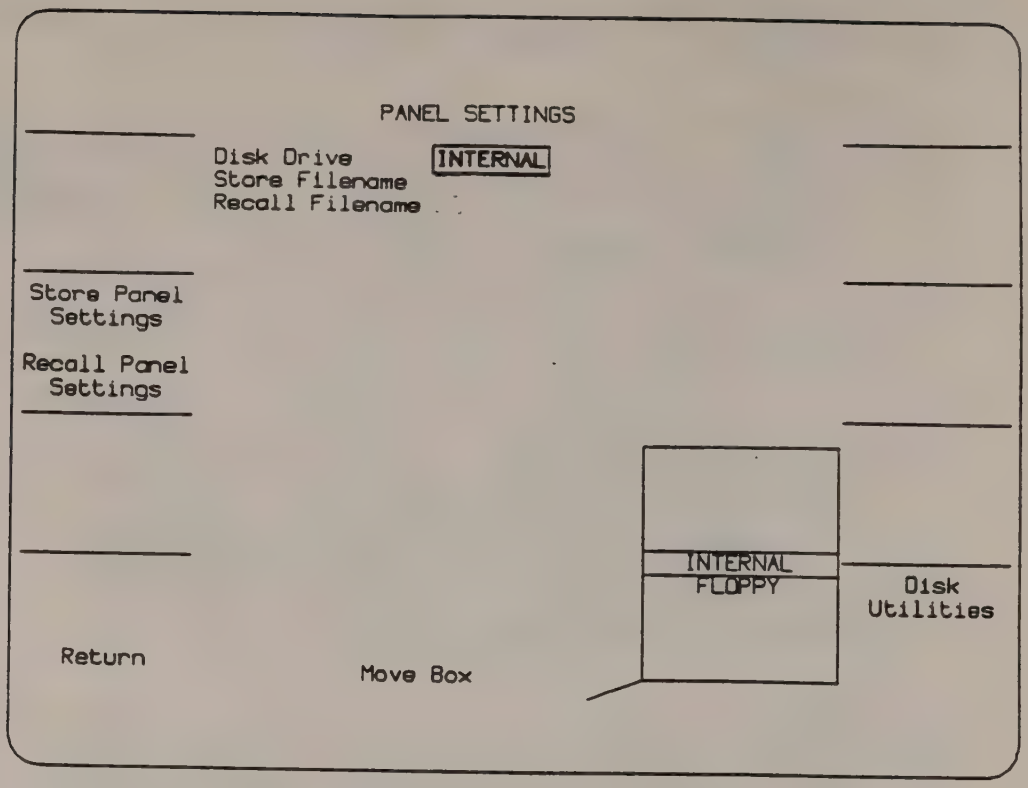


Figure 2-9. Panel Settings Screen

d. Press **MODIFY** key and **RUN PROGRAM** softkey.

e. Rotate **Move Box** knob to highlight Disk in move select box.

f. Rotate **MODIFY VALUE** knob to select **Floppy**. The screen will resemble figure 2-5.

g. Press **Recall Filename** softkey to recall filename **ADC**

h. Press **Recall** softkey.

i. Press **Return** softkey (see figure 2-4).

2-5.2 Test Procedure

a. Press **Run ADC** softkey. Panel settings shown in figure 2-9 will be recalled, then program will increment offset through ± 80 % of full scale in 10 mv steps at each of three sampling configurations. Each of three time bases tested will be checked at 35 levels for both CH1 and CH2.

If standard deviation at any level exceeds 3 mV, number of failed tests will be incremented.

2-5.3 Test Results

When all three configurations have been tested, program will display results shown in figure 2-10.

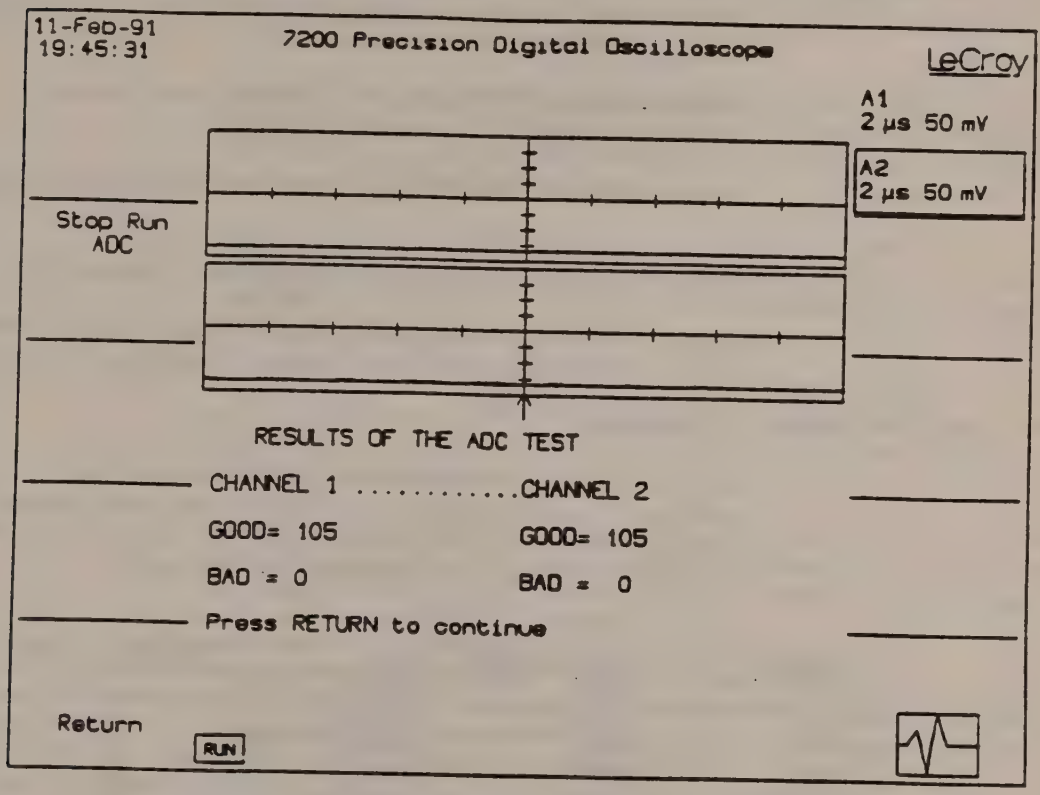


Figure 2-10. ADC Test Results (Typical)

b. Press Return softkey to terminate ADC test.

2-6 Input Impedance Test

The purpose of this test is to determine whether input impedance remains within ± 2% of 50 ohms as gain is varied between 5 mV/div and 1000 mV/div.

2-6.1 Test Setup

a. Connect DVM to BNC connector of channel under test.

b. At front panel of 7200 Mainframe, press **Configure System** softkey. You should see a screen that resembles figure 2-4.

c. Press **Panel Settings** softkey. You should see a screen that resembles figure 2-9.

d. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

e. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **IMPED**.

f. Press **Recall Panel Settings** softkey (see figure 2-9).

g. Press **Yes** softkey (not shown in figure 2-9).

h. Press **Return** softkey twice. This will recall the panel settings for the input impedance test.

2-6.2 Test Procedure

a. Rotate outer **V/DIV** knob (8, figure A-1) to select gain of 5 millivolts per division and check display for input impedance level of 50 ohms ± 2%. Mark box in figure 2-11 if impedance correct.

Channel	Vertical Coupling	Gain	Input Z is 50 +/-2%
CH1	50 DC	5mV/div	☐
CH1	50 DC	10mV/div	☐
CH1	50 DC	20mV/div	☐
CH1	50 DC	50mV/div	☐
CH1	50 DC	100mV/div	☐
CH1	50 DC	200mV/div	☐
CH1	50 DC	500mV/div	☐
CH1	50 DC	1000mV/div	☐
CH2	50 DC	5mV/div	☐
CH2	50 DC	10mV/div	☐
CH2	50 DC	20mV/div	☐
CH2	50 DC	50mV.div	☐
CH2	50 DC	100mV/div	☐
CH2	50 DC	200mV/div	☐
CH2	50 DC	500mV/div	☐
CH2	50 DC	1000mV/div	☐

The limits for the 50 ohm input impedance test are between 49ohms - 51 ohms

Figure 2-11. Impedance Test Results - 50 Ohm

b. Rotate outer **V/DIV** knob to select gain of 10 millivolts per division and check display for input impedance level of 50 ohms ± 2%. Mark box in figure 2-11 if impedance correct.

c. Rotate outer **V/DIV** knob to select gain of 20 millivolts per division and check display for input impedance level of 50 ohms ± 2%. Mark box in figure 2-11 if impedance correct.

d. Rotate outer **V/DIV** knob to select gain of 50 millivolts per division and check display for input impedance level of 50 ohms ± 2%. Mark box in figure 2-11 if impedance correct.

e. Rotate outer **V/DIV** knob to select gain of 100 millivolts per division and check display for input impedance level of 50 ohms ± 2%. Mark box in figure 2-11 if impedance correct.

f. Rotate outer **V/DIV** knob to select gain of 200 millivolts per division and check display for input impedance level of 50 ohms ± 2%. Mark box in figure 2-11 if impedance correct.

g. Rotate outer **V/DIV** knob to select gain of 500 millivolts per division and check display for input impedance level of 50 ohms ± 2%. Mark box in figure 2-11 if impedance correct.

h. Rotate outer **V/DIV** knob to select gain of 1000 millivolts per division and check display for input impedance level of 50 ohms ± 2%. Mark box in figure 2-11 if impedance correct.

i. Press upper **TRIGGER SOURCE** key (3) to switch from channel 1 to channel 2. Repeat steps a. through h.

j. Press lower **VERTICAL COUPLING** key (15) twice to change input impedance of both channels to 1 megohm.

k. Rotate outer **V/DIV** knob (8) to select gain of 5 millivolts per division and check display for input impedance level of 1 megohm ± 2%. Mark box in figure 2-12 if impedance correct.

l. Rotate outer **V/DIV** knob to select gain of 10 millivolts per division and check display for input impedance level of 1 megohm ± 2%. Mark box in figure 2-12 if impedance correct.

Channel	Vertical Coupling	Gain	Input Z is 1M +/-2%
CH1	1 MOhm DC	5mV/div	☐
CH1	1 MOhm DC	10mV/div	☐
CH1	1 MOhm DC	20mV/div	☐
CH1	1 MOhm DC	50mV/div	☐
CH1	1 MOhm DC	100mV/div	☐
CH1	1 MOhm DC	200mV/div	☐
CH1	1 MOhm DC	500mV/div	☐
CH1	1 MOhm DC	1000mV/div	☐
CH2	1 MOhm DC	5mV/div	☐
CH2	1 MOhm DC	10mV/div	☐
CH2	1 MOhm DC	20mV/div	☐
CH2	1 MOhm DC	50mVdiv	☐
CH2	1 MOhm DC	100mV/div	☐
CH2	1 MOhm DC	200mV/div	☐
CH2	1 MOhm DC	500mV/div	☐
CH2	1 MOhm DC	1000mV/div	☐

Figure 2-12. Impedance Test Results - 1 Megohm

m. Rotate outer **V/DIV** knob (8) to select gain of 20 millivolts per division and check display for input impedance level of 1 megohm ± 2%. Mark box in figure 2-12 if impedance correct.

n. Rotate outer **V/DIV** knob to select gain of 50 millivolts per division and check display for input impedance level of 1 megohm ± 2%. Mark box in figure 2-12 if impedance correct.

o. Rotate outer **V/DIV** knob to select gain of 100 millivolts per division and check display for input impedance level of 1 megohm ± 2%. Mark box in figure 2-12 if impedance correct.

p. Rotate outer **V/DIV** knob to select gain of 200 millivolts per division and check display for input impedance level of 1 megohm ± 2%. Mark box in figure 2-12 if impedance correct.

q. Rotate outer **V/DIV** knob to select gain of 500 millivolts per division and check display for input impedance level of 1 megohm ± 2%. Mark box in figure 2-12 if impedance correct.

r. Rotate outer **V/DIV** knob to select gain of 1000 millivolts per division and check display for input impedance level of 1 megohm ± 2%. Mark box in figure 2-12 if impedance correct.

s. Press upper **TRIGGER SOURCE** key (3) to switch from channel 2 to channel 1. Repeat steps k through r.

2-6.3 Test Results

If input impedance deviates more than ± 2% from 50 ohms, the EXTR assembly is defective. Refer to chapter 4 for the removal procedure and chapter 7 for the new EXTR assembly installation procedure.

2-7 Front-End Test

The purpose of this test is to determine the front-end response of both channels to injection of a square wave.

2-7.1 Test Setup

This test requires connection of a square wave generator with a risetime ± 1 ns to channel 1. Use the following setup procedure:

a. At front panel of 7200 Mainframe, press **Configure System** softkey. You should see a screen that resembles figure 2-4.

b. Press **PANEL SETTINGS** softkey. You should see a screen that resembles figure 2-9.

c. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

d. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **OVERSHOT1**.

e. Press **Recall Panel Settings** softkey (see figure 2-9).

f. Press **Yes** softkey.

g. Press **Return** softkey twice. The channel 1 panel settings shown in figure 2-13 will be recalled.

h. Connect generator to CH1 connector on front panel of 7242 Plug-In Module.

i. Turn on generator. Set input frequency to 5.0 MHz and adjust amplitude to produce 600 millivolt p-p square wave.

Trace 1	on
Grid	single
Input Coupling	50 DC
Input Gain	100 mV/div
Offset	ZERO
Time/div	50ns
Trigger:	
SMART(COMPLEX) Trigger:	OFF
Source:	CH1
Coupling:	DC
Coupling:	DC
Mode:	NORM
Delay:	ZERO
Level:	ZERO
BWL:	OFF

Extended parameters are as follows:

T1:OVSP T2:OVSN

T1:AMPL T2:FREQ

Figure 2-13. Front End Test Panel Settings - CH 1

2-7.2 Test Procedure

a. Displayed waveform should resemble figure 2-14.

b. At front panel of 7242 Plug-In Module, rotate outer **V/DIV** knob (8, figure A-1) to select 60 millivolts of gain per division.

c. Rotate outer **V/DIV** knob to select 10 millivolts p-p of gain per division. Observe display for <10% overshoot on rising and falling edges of waveform as shown in figure 2-15.

d. Turn off square wave generator and disconnect from channel 1.

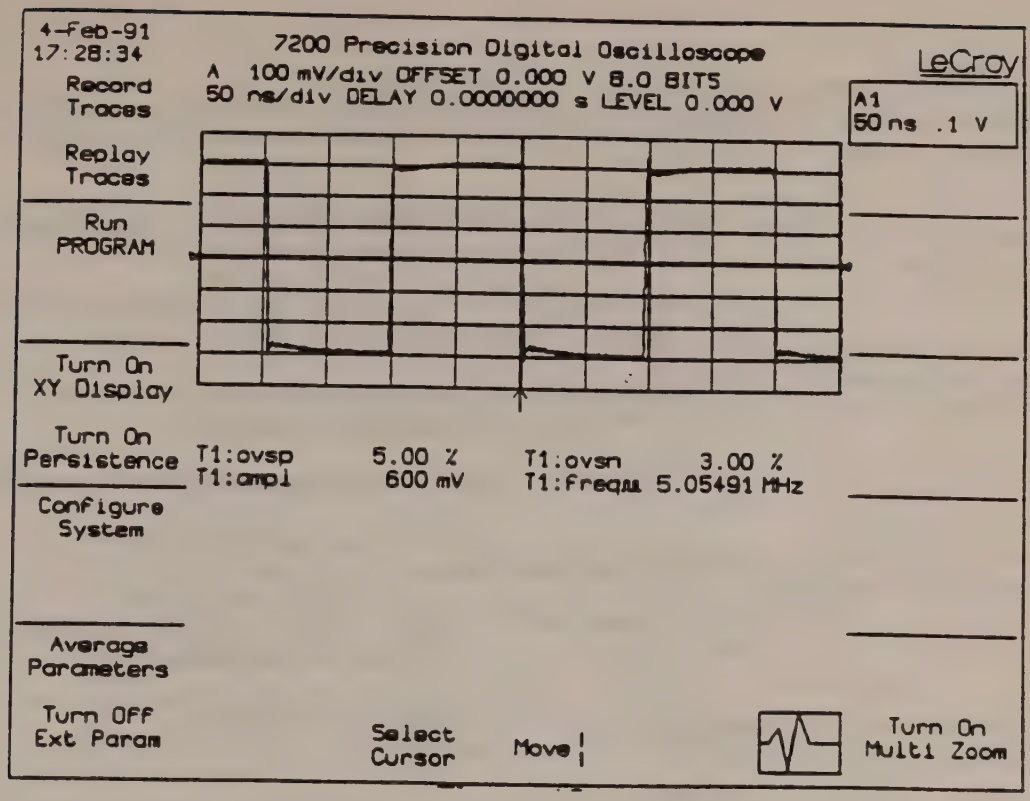


Figure 2-14. Overshoot at 600 mV p-p

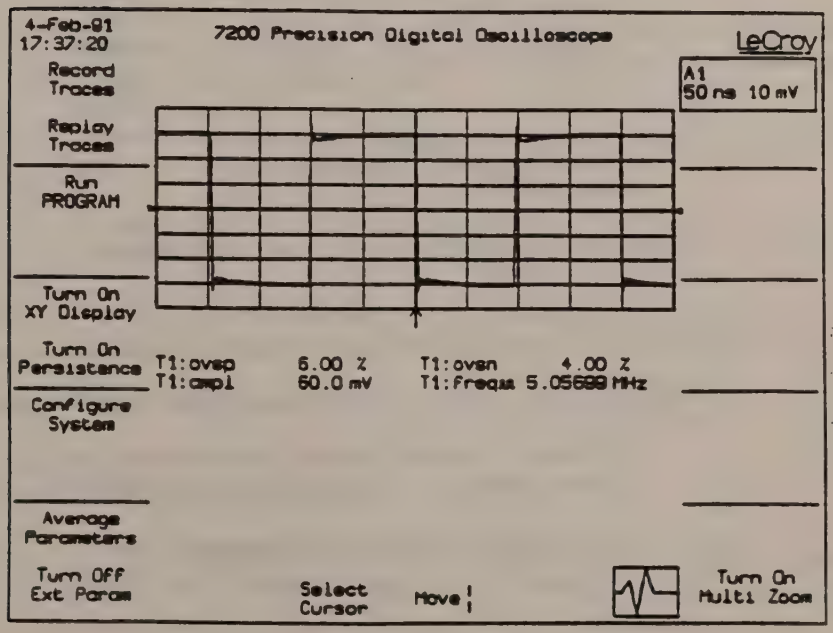


Figure 2-15. Overshoot at 60mV/Div

e. At front panel of 7200 mainframe, press **Configure System** softkey. You should see screen that resembles figure 2-4.

f. Press **PANEL SETTINGS** softkey. You should see a screen that resembles figure 2-9.

g. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

h. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **ovrshot2**.

i. Press **Recall Panel Settings** softkey (see figure 2-9)

j. Press **Yes** softkey.

k. Press **Return** softkey twice. The panel settings shown in figure 2-16 will be recalled.

Trace 1 on

Grid single

Input 50 ohms, gain 100mV/div, offset zero

Trigger:

SMART (COMPLEX) Trigger:	OFF
Source:	CH2
Coupling:	DC
Mode:	NORM
Level:	zero

Time/div = 50ns/div
BWL OFF

Extended parameters are as follows:

T1:ovsp T2:ovsn

Figure 2-16. Front-End Test Panel Settings - CH 2

l. Connect square wave generator to CH2 connector on front panel of 7242 Plug-In Module.

m. Press **CH2** key (12, figure A-1).

n. Turn on generator. Set input frequency to 5.0 MHz and adjust amplitude to produce 600 millivolt p-p square wave. Displayed waveform should resemble figure 2-14.

o. At front panel of 7242 Plug-In Module, rotate outer **V/DIV** knob (8, figure A-1) to select 60 millivolts of gain per division.

p. Rotate outer **V/DIV** knob to select 10 millivolts p-p of gain per division. Observe display for <10% overshoot on rising and falling edges of waveform as shown in figure 2-15.

2-7.3 Test Results

If there is more than 10% overshoot on the rising or falling edge of any waveform observed on the display of the 7200 Mainframe, repair is necessary.

2-8 Trigger Delay Test

The purpose of this test is to determine the rise and fall time of a square wave in relation to a trigger pulse.

2-8.1 Channel 1 Test Setup

To set up the channel 1 trigger delay test, use the following procedure:

a. At front panel of 7200 Mainframe, press **Configure System** softkey. You should see a screen that resembles figure 2-4.

b. Press **Panel Settings** softkey. You should see a screen that resembles figure 2-9.

c. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

d. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **DELAY1**.

e. Press **Recall Panel Settings** softkey (see figure 2-9).

f. Press **Yes** softkey.

g. Press **Return** softkey twice. This will recall the panel settings shown in figure 2-17.

Trace 1:	on
Grid:	single
Input couplings CH1 and CH2:	50 DC
Input gain:	200mV/div
Time/div:	2ns
Trigger:	
SMART(COMPLEX)Trigger:	OFF
Source:	CH1
Coupling:	DC
Level:	ZERO
Mode:	NORM

Extended parameters are as follows:

T1:tafl T1:tars

T1:ampl T1:freq

Figure 2-17. Trigger Delay Test Panel Settings - CH1

2-8.2 Channel 1 Test Procedure

Press SLOPE key (19, figure A-1) to select POS. Record TARS (limit is ± 1 ns).

Press SLOPE key to select NEG. Record TAFL (limit is ± 1 ns).

2-8.3 Channel 1 Test Results

TARS ≤ 1 ns

TAFL ≤ 1 ns

Results are expressed in terms of time after rise (TARS) for a positive-sloping trigger pulse, and time after fall (TAFL) for a negative-sloping trigger pulse.

2-8.4 Channel 2 Test Setup

To set up the channel 2 trigger delay test, use the following procedure:

a. At front panel of 7200 Mainframe, press Configure System softkey. You should see a screen that resembles figure 2-4.

b. Press **Panel Settings** softkey. You should see a screen that resembles figure 2-9.

c. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

d. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **DELAY2**.

e. Press **Recall Panel Settings** softkey (see figure 2-6).

f. Press **Yes** softkey.

g. Press **Return** softkey twice. This will recall the panel settings shown in figure 2-18.

Trace 1 on

Grid single

Input couplings CH1 and CH2: 50 ohms

Input gain .2mV/div

Time/div = 20ns

Trigger:

SMART (COMPLEX) Trigger:	OFF
Source:	CH2
Coupling:	DC
Level:	zero
Mode:	NORM

Extended parameters for CH2 are as follows:

T1:tafl	T1:tars
T1:ampl	T1:freq

Figure 2-18. Trigger Delay Test Panel Settings - CH 2

2-8.5 Channel 2 Test Procedure

a. Press **SLOPE** key (19, figure A-1) to select **POS**. Record **TARS**.

b. Press **SLOPE** key to select **NEG**. Record **TAFL**.

2-8.6 Channel 2 Test Results

TARS ≤ 1 ns

TAFL ≤ 1 ns

Results are expressed in terms of time after rise (TARS) for a positive-sloping trigger pulse, and time after fall (TAFL) for a negative-sloping trigger pulse.

2-9 Bandwidth Test

The purpose of this test is to determine bandwidth at frequencies ranging from 1 MHz to 200 MHz by measuring standard deviation.

2-9.1 Channel 1 Test Setup

This test requires a calibrated sine wave generator capable of producing a 1 MHz signal. To set up the bandwidth test, use the following procedure:

a. At front panel of 7242 Plug-In Module, connect generator to CH 1 connector.

b. Turn on generator and set to produce 1 MHz output.

c. Adjust amplitude to 100 mv sdev.

d. At front panel of 7200 Mainframe, press **Configure System** softkey. You should see a display that resembles figure 2-4.

e. Press **Panel Settings** softkey. You should see a display that resembles figure 2-9.

f. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

g. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **BWCH1**.

h. Press **Recall Panel Settings** softkey (see figure 2-9).

i. Press **Yes** softkey.

j. Press **Return** softkey twice. This will recall the panel settings shown in figure 2-19.

2-9.2 Channel 1 Test Procedure

a. Slowly increase generator frequency until T1:rms=100.0 mv (approximately -7.2 dB) as shown in figure 2-20.

b. Slowly increase frequency of sine wave generator until T1:freq=200 MHz. Observe that T1:RMS does not drop below 70.7 millivolts between 1 MHz and 200 MHz.

Trace 1	on
Grid	single
Input couplings CH1 and CH2:	50 DC Input gain 50mV/div
Time/div	2us
Trigger:	
SMART(COMPLEX)Trigger:	OFF
Source:	CH1
Coupling:	DC
Level:	ZERO
Mode:	NORM
Memory:	20K

Extended parameters are as follows:

T1:sdev T1:freq

Figure 2-19. Bandwidth Test Settings - CH 1

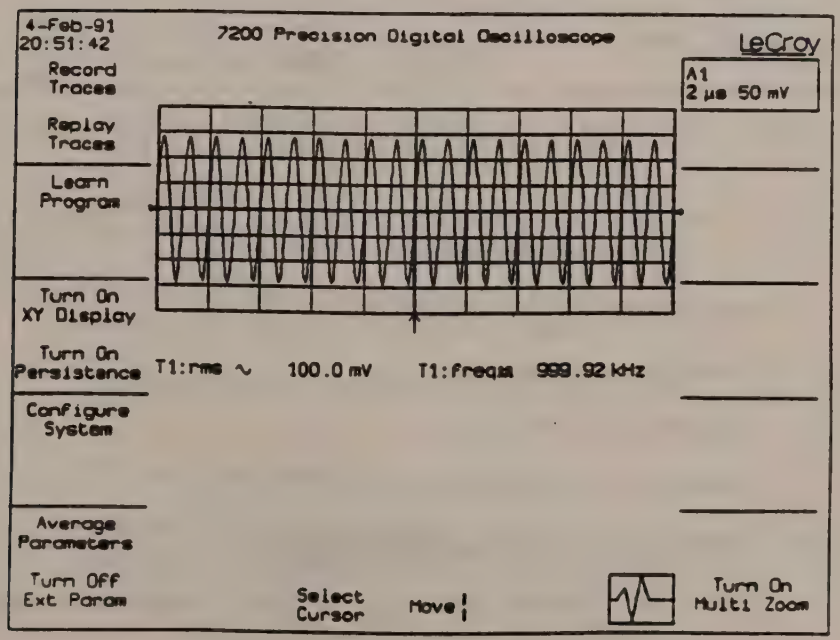


Figure 2-20. T1:RMS Amplitude

b. At front panel of 7242 Plug-In Module, rotate **TIMEBASE** knob (1, figure A-1) to set t/div to 20 ns.

c. Press **INTERLEAVED SAMPLING** button (2) to stabilize readout of T1:sdev and T1:freq on display (see figure 2-21).

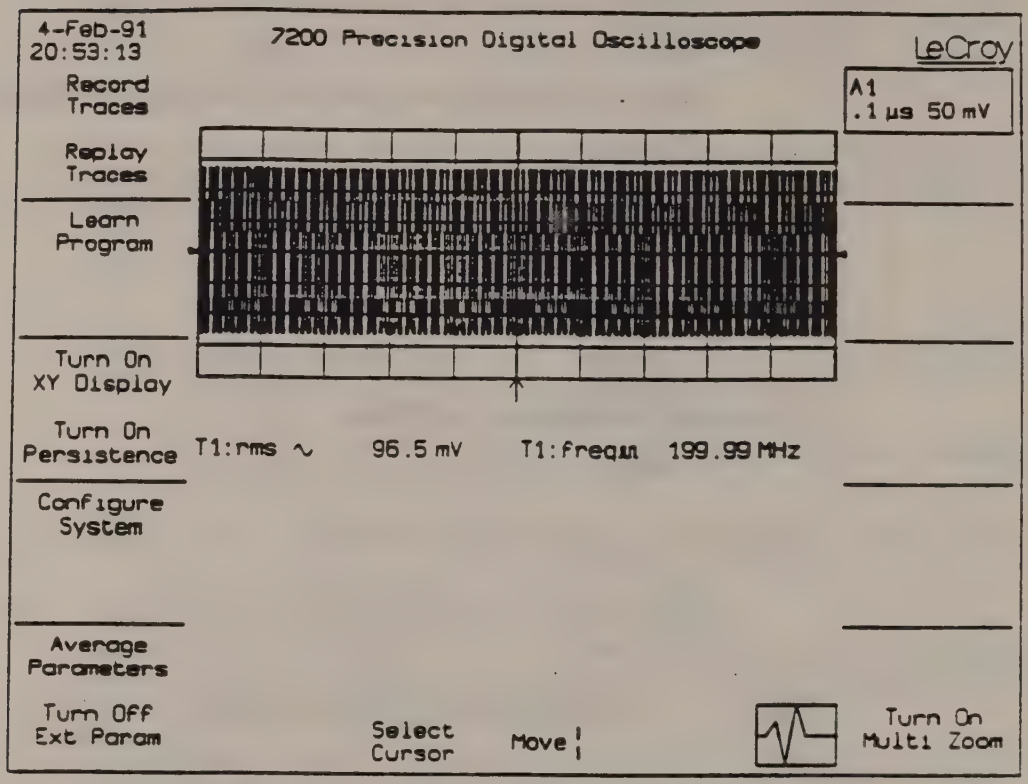


Figure 2-21. RIS Enabled at 200 MHz

d. Continue to increase frequency until T1:FREQ=400 MHz as shown in figure 2-22. Record T1:RMS when T1:FREQ=400 MHz.

e. Turn off generator.

2-9.3 Channel 1 Test Results

T1:RMS = ≥ 70.7 mV

2-9.4 Channel 2 Test Setup

Use the following procedure:

a. At front panel of 7242 Plug-In Module, connect generator to CH 2 connector.

b. Turn on generator and set to produce 1 MHz output.

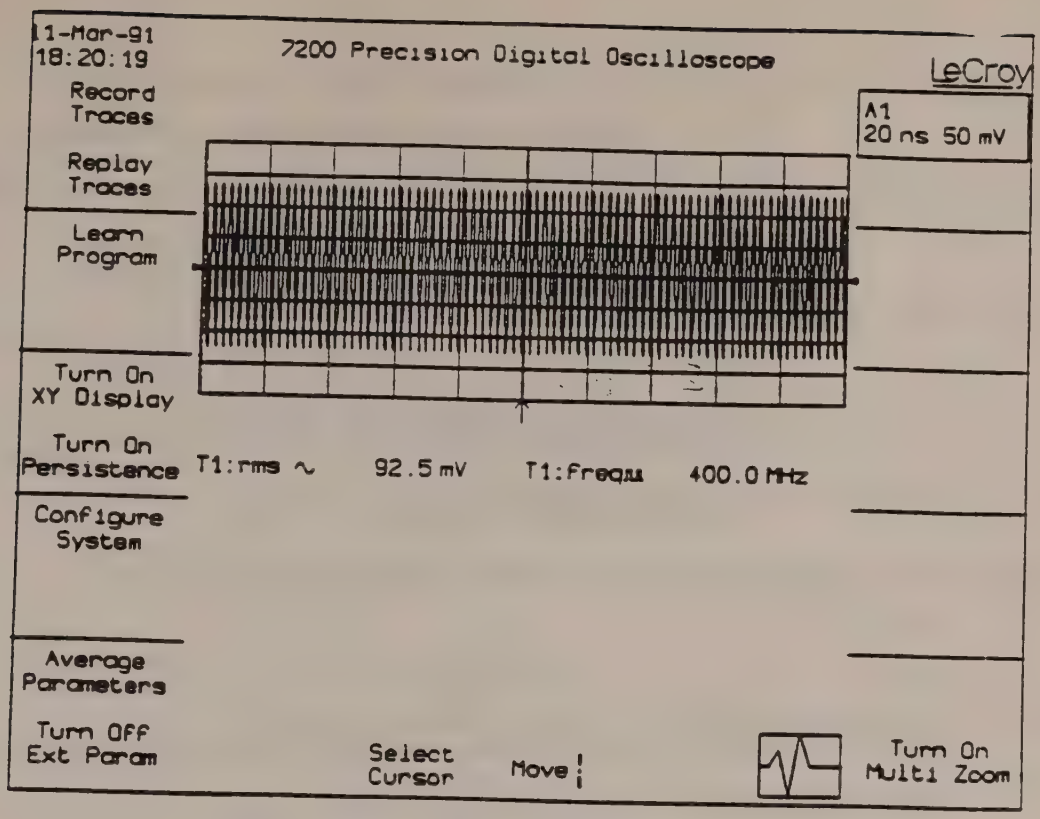


Figure 2-22. RMS Voltage at 400 MHZ

c. Adjust amplitude until T1:rms= 100.0 mv.

d. At front panel of 7200 Mainframe, press Configure System softkey. You should see a display that resembles figure 2-4.

e. Press Panel Settings softkey. You should see a display that resembles figure 2-9.

f. Press Disk Drive softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

g. Press Recall Filename softkey (not shown in figure 2-9) to select filename **BWCH1**.

h. Press Recall Panel Settings softkey (see figure 2-9).

i. Press Yes softkey.

j. Press Return softkey twice. This will recall the panel settings shown in figure 2-23.

2-9.5 Channel 2 Test Procedure

a. Slowly increase sine wave generator frequency until T2:freq=200 MHz. Observe that T2:RMS does not drop below 70.7 millivolts between 1 MHz and 200 MHz.

b. At front panel of 7242 Plug-In Module, rotate **TIMEBASE** knob (1) to set T/DIV to 20 ns.

c. Press **INTERLEAVED SAMPLING** button (2) to stabilize readout of T1:RMS and T1:freq on display.

d. At generator, continue to increase frequency until T2:FREQ=400 MHz. Record T2:RMS when T2:FREQ=400 MHz.

e. Turn off generator.

Trace 1 on

Grid single

Input couplings CH1 and CH2: 50 ohms DC Input gain 50mV/div

Time/div = 2us

Trigger:

SMART (COMPLEX) Trigger:	OFF
Source:	CH2
Coupling:	DC
Level:	zero
Mode:	NORM
Memory	20K

Extended parameters are as follows:

T1:sdev T1:freq

Figure 2-23. Bandwidth Test Panel Settings - CH 2

2-9.6 Channel 2 Test Results

T2:RMS = ≥ 70.7 mV

2-10 DC Gain and Linearity Test

The purpose of this test is to determine DC gain and linearity in response to a 1 KHz bipolar square wave centered about 0 VDC as the input level is varied between 30 mv p-p and 3 v p-p.

2-10.1 Channel 1 Test Setup

Use the following procedure:

a. At front panel of 7200 Mainframe, press **Configure System** softkey. You should see a screen that resembles figure 2-4.

b. Press **Panel Settings** softkey. You should see a screen that resembles figure 2-9.

c. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

d. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **DCLIN**.

e. Press **Recall Panel Settings** softkey (see figure 2-9).

f. Press **Return** softkey.

g. Press **RUN DCLIN** softkey. This will recall the panel settings shown in figure 2-24.

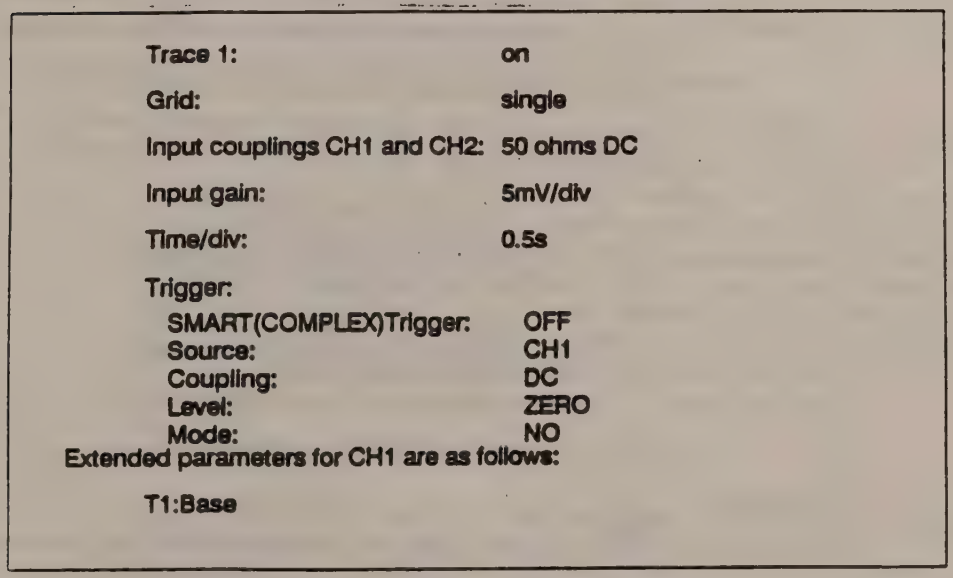


Figure 2-24. DC Gain and Linearity Test Panel Settings - CH 1

2-10.2 Channel 1 Test Procedure

a. This test requires a precision DC supply. To set up the channel 1 DC gain and linearity test, use the following procedure:

b. At front panel of 7242 Plug-In Module, connect DC supply to CH 1 BNC connector.

c. Press Return softkey.

d. Turn on DC supply and set output level to 15 mv. The 7200 Mainframe calculates the average base value for 100 sweeps of 2000 points each (200,000 points). After each step of the test, output similar to figure 2-25 is displayed. The data display indicates whether the previous test was **PASSED**, the lower limit, the upper limit, the actual voltage, which voltage range is to be tested next, and the input voltage the DC supply is to be set to.

e. Press Return softkey to continue.

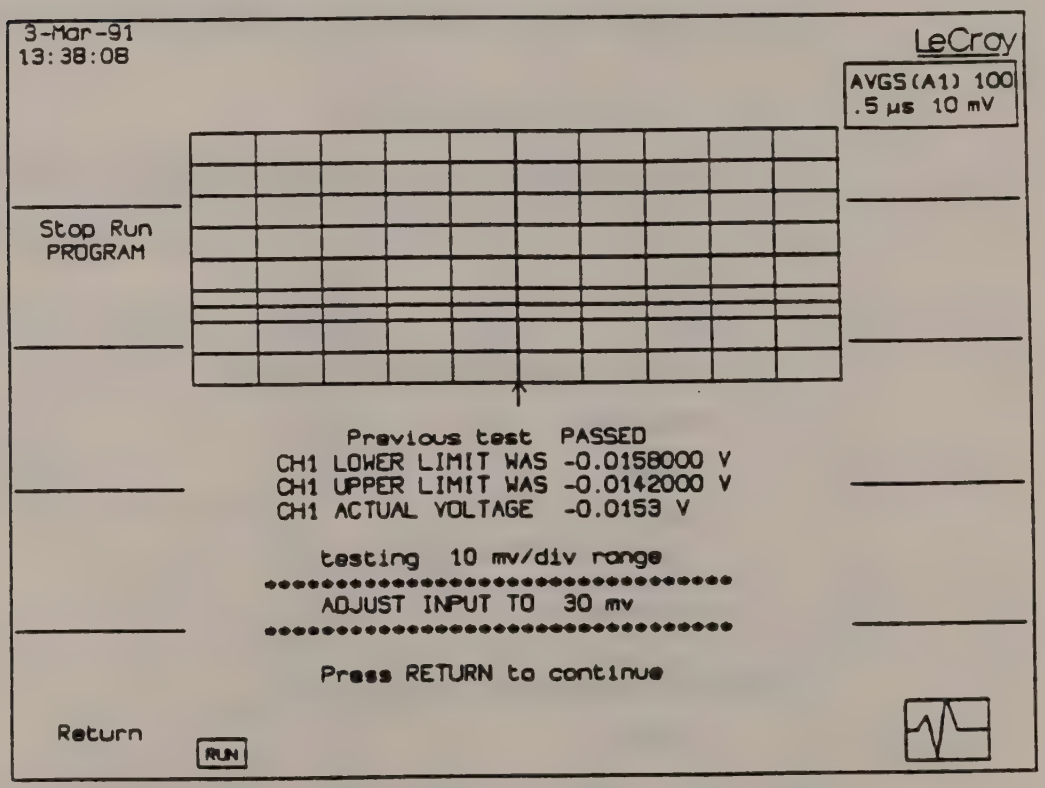


Figure 2-25. Test Status and Parameters

f. Repeat testing until **CONNECT PRECISION DC SUPPLY TO CH 2 INPUT** message displayed (see figure 2-26).

g. Turn off precision DC supply, disconnect from CH1 and connect to CH 2.

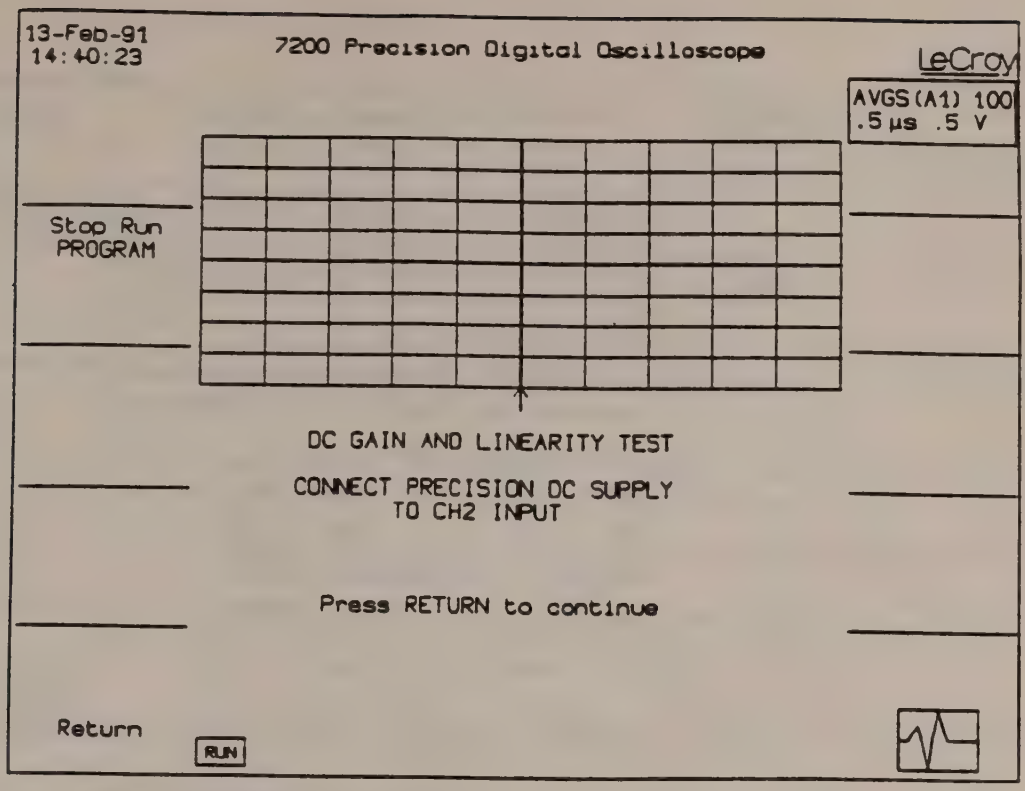


Figure 2-26. Channel Change Message

h. Turn on precision DC supply and set output to level indicated. 7200 Mainframe again calculates the average base value for 100 sweeps of 2000 points each (200,000 points). After each step of the test, output similar to figure 2-26 is displayed. The data display indicates whether the previous test was **PASSED**, the lower limit, the upper limit, the actual voltage, which voltage range is to be tested next, and the input voltage the precision DC supply is to be set to.

i. Press **Return** softkey to continue.

j. Repeat testing until **PASS** message or **FAILED** message displayed as in figure 2-27.

2-10.3 Test Results

If the output at any step of the test procedure is above or below the specified range by 2% or more, pressing the **Return** softkey will cause a list of errors to be displayed (see figure 2-27).

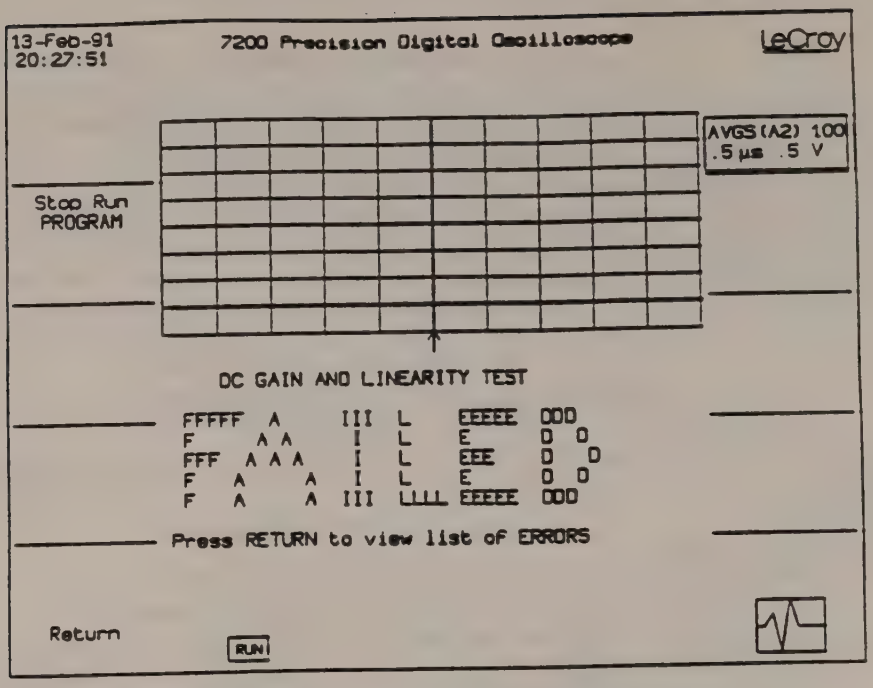

13-Feb-91
20:27:51
7200 Precision Digital Oscilloscope
LeCroy
AVGS(A2) 100
.5 µs .5 V
Stop Run
PROGRAM
DC GAIN AND LINEARITY TEST
FFFFF A III L EEEEE 000
F A A I L E 0 0
FFF A A A I L EEE 0 0
F A A I L E 0 0
F A A III LLLL EEEEE 000
Press RETURN to view list of ERRORS
Return
RUN

Figure 2-27. Test Failure Display

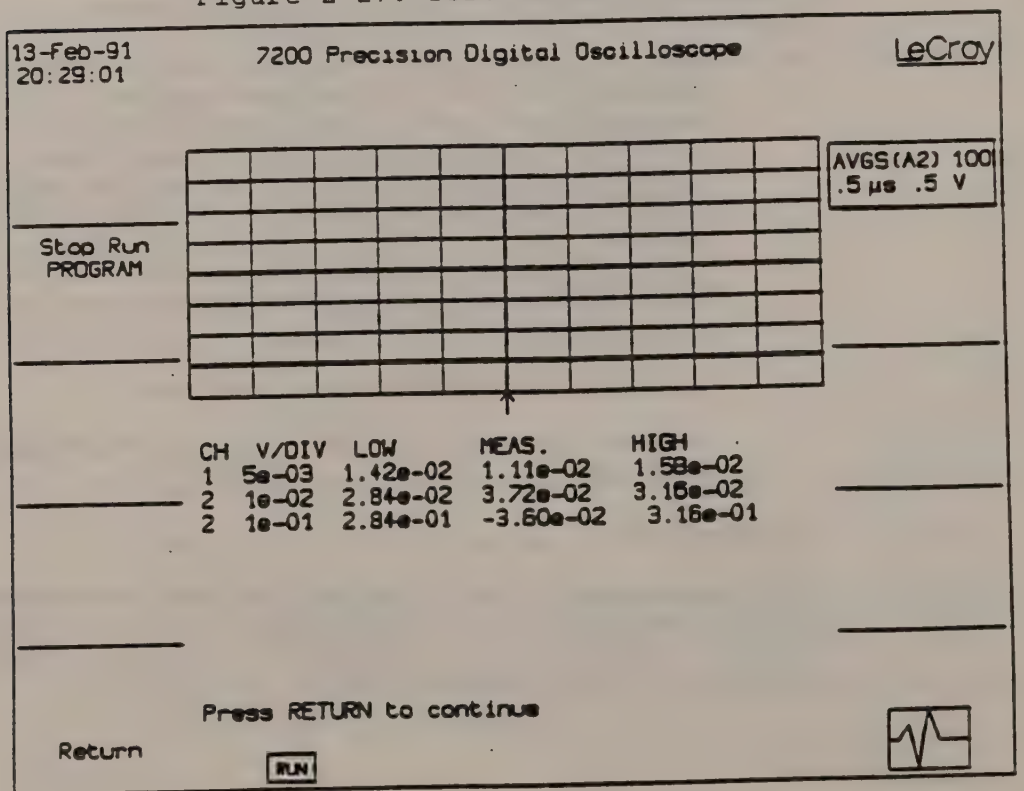


Figure 2-28. Error List

2-11 Trigger Accuracy Test

2-11.1 Test Setup

a. Connect sine wave generator to CH 1 BNC connector on front panel of Module. Set input frequency to 10 KHz and amplitude to 1.5 v p-p.

b. On 7200 Mainframe, press **MODIFY** key and **RUN DCLIN** softkey.

c. At front panel of 7200 Mainframe, press **Configure System** softkey. You should see a display that resembles figure 2-4.

d. Press **Panel Settings** softkey. You should see a display that resembles figure 2-9.

e. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

f. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **TRIGLEV**.

g. Press **Recall Panel Settings** softkey (see figure 2-9).

h. Press **Return** softkey.

2-11.2 Test Procedure

a. Press **RUN TRIGLEV** softkey. Program tests the accuracy of the CH 1 trigger level circuit in the 200 mv/div range. Test limits are based on the following criteria:

RANGE = ± 5*(v/div) = ± 5*200 mV = ± 1 volt

RESOLUTION = 0.025% of range = 0.00025 * 1 volt = 250 V

ACCURACY = ± 5% of range = ± 50 mV

When testing of channel 1 is complete, a **Test of CH1 PASSED** message is displayed as shown in figure 2-28 or a **FAILED** message is displayed.

b. Turn off sine wave generator and disconnect from channel 1 BNC connector. Connect to CH 2 BNC connector and turn on.

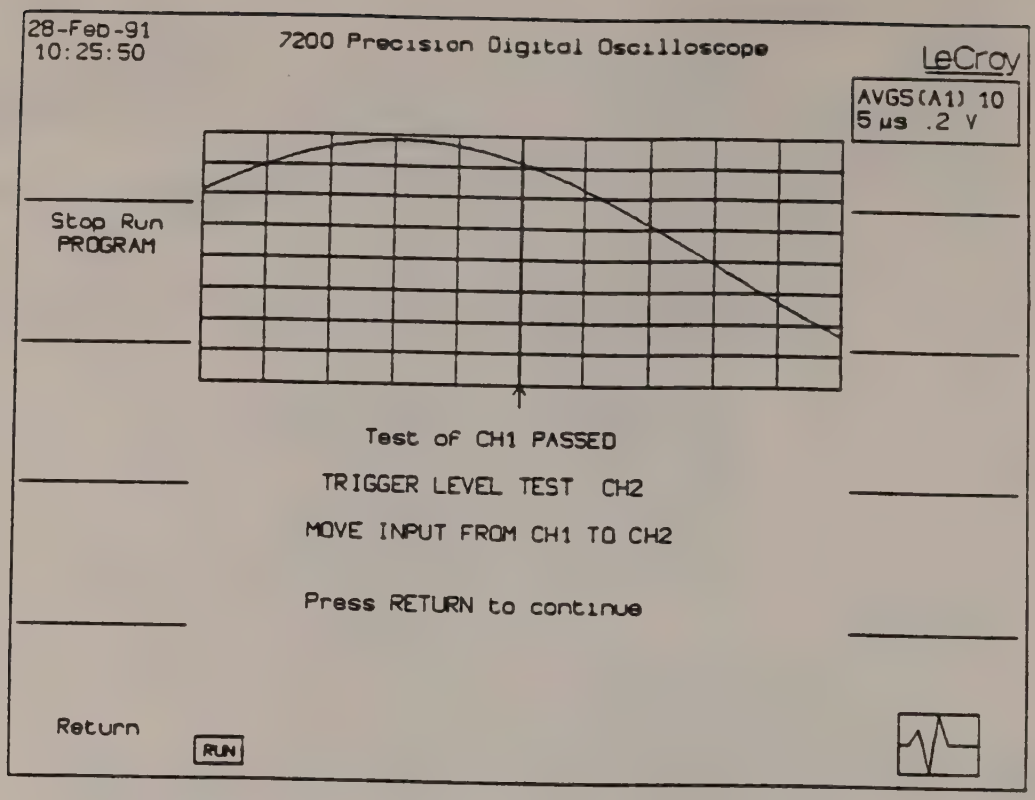


Figure 2-28. Channel 1 Test Completion

c. Press **Return** softkey. The program tests the accuracy of the CH 2 trigger level circuit in the 200 mv/div range. When testing of channel 2 is complete, a **Test of CH2 PASSED** message similar to the one shown in figure 2-28 is displayed or a **FAILED** message is displayed.

d. Turn off sine wave generator and disconnect from channel 2 BNC connector. Connect sine wave generator to BNC "T" connector connected to external trigger connector. Use short length of coaxial cable to connect CH2 BNC connector to BNC "T" connector.

e. Press **Return** softkey to continue testing.

2-11.3 Test Results

When channel 2 testing is complete, a screen similar to figure 2-28 is displayed. If logging was enabled, the logged data show that the trigger level was set in 100 mV increments between -600 mV and +600 mV and the actual voltage level measured at trigger time was expected to be within ± 50 mV of the set level. Positive slope, negative slope, and external triggers were tested on both channels. Results outside of these limits are marked as failed on the test results.

2-12 Time Base Accuracy Test

The purpose of this test is to verify the time base through use of a sine wave signal generator with a frequency accuracy of 1 ppm or less.

2-12.1 Test Setup

a. At front panel of 7200 Mainframe, press **Configure System** softkey. You should see a screen that resembles figure 2-4.

b. Press **Panel Settings** softkey. You should see a screen that resembles figure 2-9.

c. Press **Disk Drive** softkey (not shown in figure 2-9) to select disk drive **FLOPPY**.

d. Press **Recall Filename** softkey (not shown in figure 2-9) to select filename **TIMEBASE**.

e. Press **Yes** softkey.

f. Press **Return Softkey** twice. This wil recall timebase accuracy test panel settings (figure 2-29).

g. Connect sine wave generator to CH1 input.

h. Adjust input frequency to 10 MHz.

i. Adjust input amplitude to 6 divisions (approximately 5.5 dB)

j. Determine whether T1:freq is less than 100 Hz as shown in figure 2-30.

Input Coupling:	50 DC
Input Gain:	200mv/div
Offset:	ZERO
Time / Div:	0.1 S
RIS:	ON
Trigger:	
SMART(COMPLEX) Trigger:	OFF
Source:	CH1
Coupling:	DC
Mode:	NORM
Slope:	POS
Delay:	ZERO
Level:	ZERO

Figure 2-29. Time Base accuracy Test Panel Settings

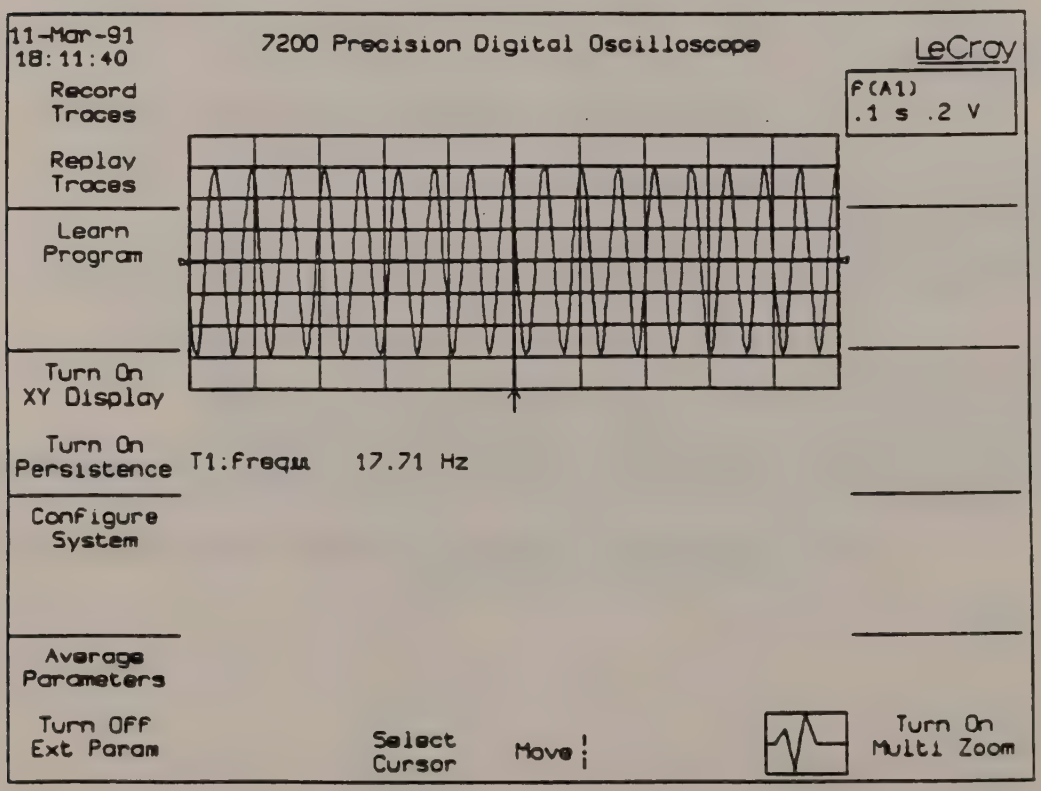


Figure 2-30. T1:FREQ = Difference Frequency

2-13 System Test

2-13.1 Introduction

A system test may be performed to identify defective Module assemblies and boards. A dongle must be installed in the Centronics port on the Rear of the 7200 Mainframe in order to access test files.

2-13.2 Test Setup

a. Insert ATE install disk 1 (of 3) into floppy drive on 7200 Mainframe.

b. Apply power to 7200 Mainframe.

c. Press **Install** softkey on Front Panel assembly of 7200 Mainframe, then **Start** softkey.

d. Follow screen prompts for disks 2 and 3.

e. Turn off 7200 Mainframe and connect dongle to Centronics port on Rear.

f. Apply power to 7200 Mainframe again and press **MODIFY** key on its Front Panel assembly, then press **Interleaved Sampling** key and **Return** softkey.

g. Press **Configure System** softkey.

NOTE

If **CANNOT READ DIRECTORY** error message is displayed, repeat steps a. through h.

2-13.3 Memory and ADC Board Test Procedure

a. Press **Disk Drive** softkey to select disk drive **INTERNAL** (see test menu screen, figure 2-31).

b. Select Model P42 to designate 7242 Plug-In Module.

c. Select appropriate subassembly, e.g., MEM(A), ADC(A), TMB.

d. Select test to run by pressing appropriate **TRACE** softkey, e.g., MEM 72XX or TEST_TMB.

e. Select Plug-In (A if Module undergoing test is in slot A or B if Module undergoing test is in slot B).

f. Select Interactive **YES**.

g. Select Iterations **1**.

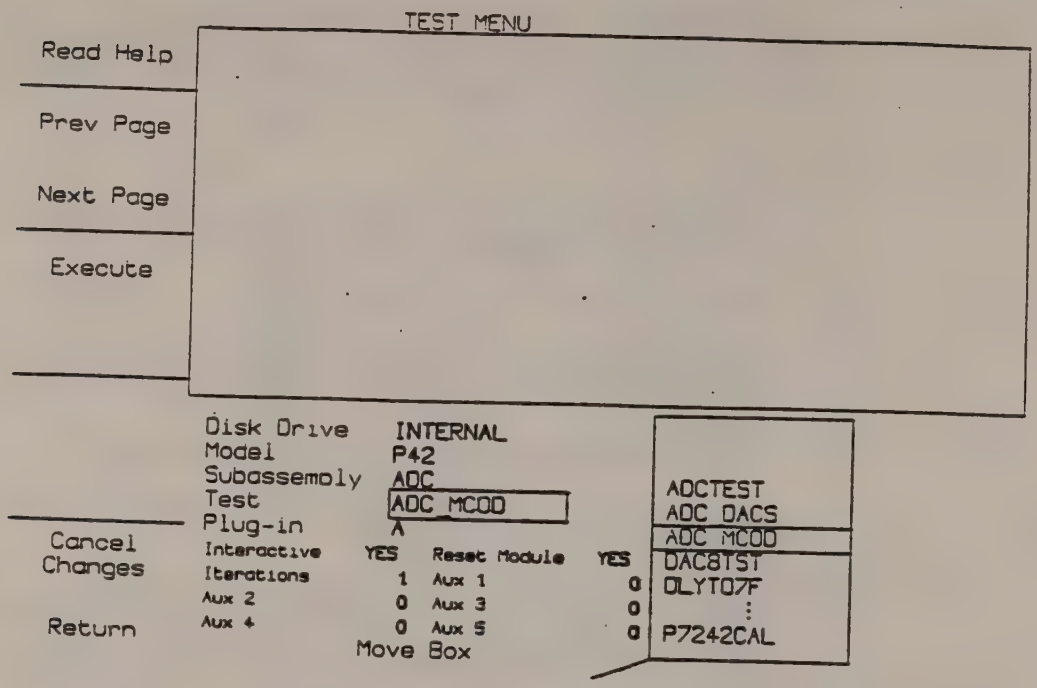


Figure 2-31. Test Menu Screen (Typical)

h. Select Reset Module YES.

i. Select Aux 1-5 0.

j. Press Execute softkey. If the MEM 72XX test was selected (Step d.), 10 test routines will be executed:

1. Data Fill
2. Data Pattern
3. Channel Isolation
4. Walking Bit A
5. Walking Bit B
6. MDX Address
7. Bank Address
8. Data = Address

9. Address

10. Phase Lock

Tests 1 through 9 are memory test routines. Test 10 exercises the phase lock loop circuitry in the ADC(A) board.

2-13.4 Memory and ADC Board Test Results

If all tests are completed successfully, a **TEST PASSED** message will be displayed; otherwise the program will stop and loop where it encounters an error. Failure of any test in the group 1 through 9 indicates a defective (or poorly seated) MEM(A) board; Failure of test 10 indicates a defective (or poorly seated) ADC(A) board. Refer to the troubleshooting procedures in section 3 to isolate failures, and refer to sections 4 and 7 for board removal and installation.

2-13.5 TMB Board Test

This test is intended primarily for factory component level repair of TMB boards. The routine consists of toggling certain data and address lines and is useful for diagnosing board failures. Use the following procedure:

a. Select appropriate subassembly (**TMB**).

b. Select test to run by pressing appropriate TRACE softkey (**TEST_TMB**).

c. Select Plug-In (A if Module undergoing test is in slot A or B if Module undergoing test is in slot B).

d. Press **Execute** softkey once and **Yes** softkey twice to begin test. Test points A4, A25, and A26 on connector P33 are toggled.

e. To end test, press **Abort** softkey.

SECTION 3 TROUBLESHOOTING

Testing of the 7242 Plug-In Module may reveal problems which require additional troubleshooting to isolate. This section of the service manual lists 17 possible symptoms, describes them, identifies possible faults, and provides step-by step repair procedures, many with accompanying diagnostic flow diagrams. The 17 symptoms are:

Paragraph	Symptom
3-1	Bandwidth is Low
3-2	Bus Errors
3-3	Calibration Errors
3-4	Channel 1 or 2 or Both Will Not Trigger
3-5	Error Determining Module Type
3-6	Excessive Noise
3-7	External Trigger Does Not Work
3-8	Flyers (Spike Noise)
3-9	Gain Errors or Gain Incorrect
3-10	No Signal, Trace Off Screen
3-11	Offset Drifts
3-12	Plug-In Not Initialized, No Front Panel Lights
3-13	Probe Attenuation Changes Intermittently
3-14	Stuck in Calibration Mode
3-15	Time Base is Wrong
3-16	Time Base Phase Unlocked
3-17	Trigger Delay Problems

This section also includes a number of procedures and tests which are useful for trouble isolation and post-repair calibration and testing. The delay calibration procedure is included as paragraph 3-18 because it is referenced numerous times. The other procedures and tests are included in the first troubleshooting routine in which they are used, then referenced from other procedures that use the same routine.

3-1 SYMPTOM: BANDWIDTH IS LOW

DESCRIPTION:

Input signal attenuated by more than 3 dB at rated bandwidth frequency of Module. Can be confirmed by performing bandwidth test (paragraph 2-9) with BWL (bandwidth limit) off and not being displayed with signal processing (such as "ERES") on.

POSSIBLE FAULTS:

1. Defective AMP assembly

2. Defective ADC(A) board

REPAIR STEPS:

NOTE

The defective AMP assembly should be replaced with one bearing the same ECO level sticker or a higher level.

a. Replace AMP assembly (see paragraph 4-3.2 for removal of defective assembly, paragraph 7-1.4 for installation of replacement).

NOTE

Determine whether the Module contains a MEM or MEMA board. If a MEM board is used, the ADC board should be replaced with an ADC board; if a MEMA board is used, the ADC board should be replaced with an ADCA board. The ADCA board also is backwardly compatible with a MEM board if variable delay lines 4 and 5 (see appendix B, figure B-2) are 1.7 nSEC types. The defective ADC(A) board should be replaced with one bearing the same ECO level sticker or a higher level.

b. Replace ADC(A) board (see paragraph 4-3.2 for removal of defective board, paragraph 7-1.4 for installation of replacement).

c. Perform delay calibration (see paragraph 3-18).

3-2 SYMPTOM: BUS ERRORS

DESCRIPTION:

When bus error occurs, 7200 Mainframe may hang up or beep and reset. When 7200 Mainframe reinitialized after bus error has occurred, **INTERNAL SYSTEM FAULT OCCURRED** message displayed. Initialization may halt and display system fault menu or reboot normally and enter bus error in system log.

NOTE

Bus errors that occur infrequently (once a day or less) indicate a low-level system problem which may be very difficult to isolate.If errors occur infrequently, consult the factory.

POSSIBLE FAULTS:

1. Plug-In "A"
2. Plug-In "B"
3. 7200 Mainframe

REPAIR STEPS:

a. Reformat hard drive and reinstall operating system. If problem remains, go to step b.

b. Record DCFA address from bus error (see figure 3-1) Using first two or three characters from DFCA address, determine whether problem is in Plug-In "A", Plug-In "B", or 7200 Mainframe.

Address Start	Defective Assembly
08	Plug-In "A"
09	Plug-In "B"

If the starting address is 08 or 09, replace the defective Plug-In Module. All other DFCA addresses refer to specific boards in the 7200 Mainframe. Refer to the LeCroy 7000 series service manual for corrective action.

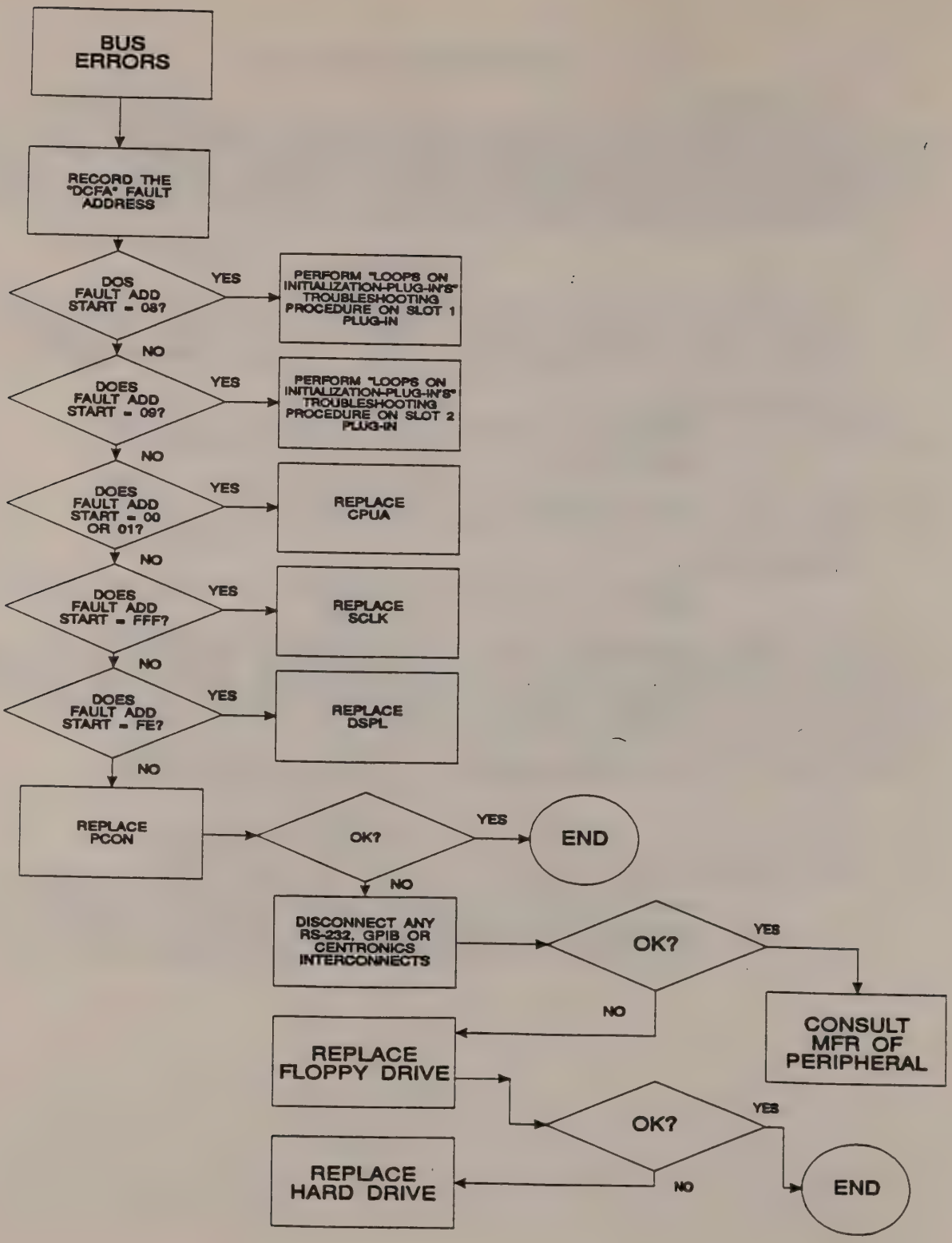


Figure 3-1. Bus Error Flow Diagram

3-3 SYMPTOM: CALIBRATION ERRORS

DESCRIPTION:

During self-calibration, 7200 Mainframe recognizes errors of five types: Dynamic Calibration, Level, Gain, TDC, and Trigger. Errors are recorded in system self-test log as shown in figure 3-2. Figure 3-3 is the calibration error flow diagram.

```
00000001 DYNAMIC CAL COULD NOT ALLOCATE MEMORY
00000002 DYNAMIC CAL COULD NOT DETERMINE FREQUENCY
00000004 DYNAMIC CAL UNREASONABLE FREQUENCY
00000008 DYNAMIC CAL ZERO POPULATION
00000010 DYNAMIC CAL COULD NOT DETERMINE PHASE
00000020 DYNAMIC CAL CLOCK IS OUT OF RANGE
00000040 PLUGIN PROCESSOR NOT RESPONDING DURING CAL
00000080 LEVEL ERROR #1
00000100 LEVEL ERROR #2
00000200 LEVEL ERROR #3
00000400 LEVEL ERROR #4
00000800 LEVEL ERROR #5
00001000 LEVEL ERROR #6
00002000 GAIN ERROR #1
00004000 GAIN ERROR #2
00008000 GAIN ERROR #3
00010000 GAIN ERROR #4
00020000 GAIN ERROR #5
00040000 GAIN ERROR #6
00080000 GAIN ERROR #7
00100000 GAIN ERROR #8
00200000 GAIN ERROR #9
00400000 TDC CAL UNBALANCED POPULATION
00800000 TDC CAL NO POSITIVE EDGE
01000000 TDC CAL NO TRANSITION
02000000 TDC CAL SMALL RANGE
04000000 TRIG LEVEL CAL ERROR
08000000 TRIG GAIN CAL ERROR
```

Figure 3-2. System Self-Test Log (Typical)

For errors 00000080 to 00200000, it should be determined whether channel is completely inoperative before correcting calibration errors.

POSSIBLE FAULTS:

1. Defective AMP assembly
2. Defective ADC(A) board
3. Defective TMB board
4. Defective MEM(A) board

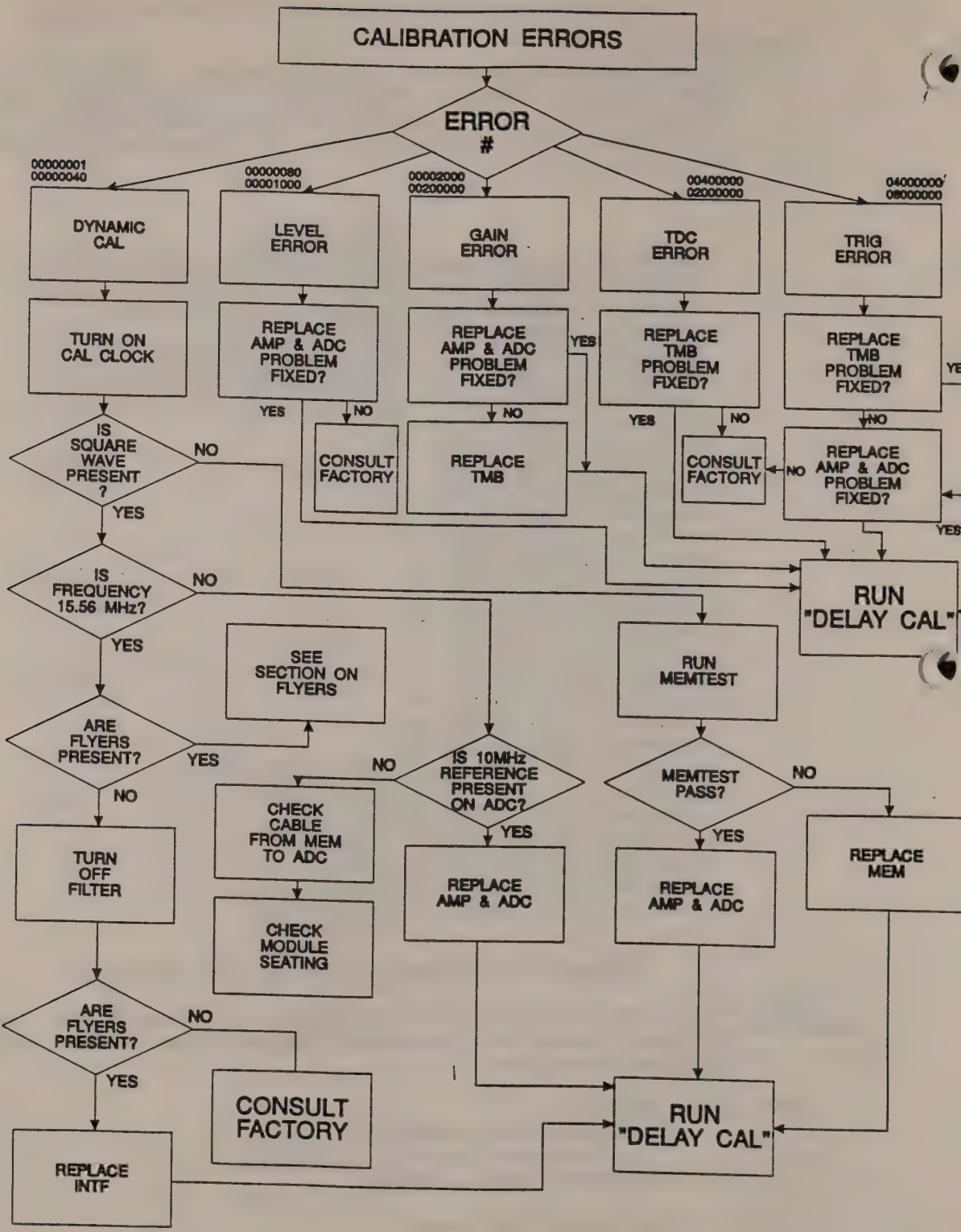


Figure 3-3. Calibration Errors Flow Diagram

REPAIR STEPS:

Refer to figure 3-3 and system self-test log to determine type of calibration error, or use calibration error (CALERR) program to decode error, then take appropriate corrective action.

Dynamic Calibration Error Correction

a. Connect dongle to Centronics port on Rear of 7200 Mainframe.

b. Apply power to 7200 Mainframe.

c. Press **MODIFY** key on Front Panel of 7200 Mainframe and **INTERLEAVED SAMPLING** key.

d. Press **CAL CLK ON** softkey and check for display of 15.56 MHZ square wave.

e. If 15.56 MHZ square wave not displayed, press **CAL CLK OFF** softkey and perform system memory test (paragraph 2-13). If test passed, replace AMP assembly and ADC(A) board (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement). If test failed, replace MEM(A) board (see paragraph 4-3.5 for removal, paragraph 7-1.1 for installation of replacement) and go to step s. If square wave displayed, verify frequency of 15.56 MHZ. If not, go to step f. If frequency 15.56 MHZ, go to step h.

f. Check for presence of 10 MHZ reference signal on ADC(A) board by placing scope probe on coax cable near **REF CLK** connector J3. If 10 MHZ REF CLK signal present, replace AMP assembly and ADC(A) board (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement pair). If **10 MHZ REF CLK** signal not present, go to step g.

g. Check coax cable that connects MEM(A) board to ADC(A) board. If cable defective or disconnected, replace or reconnect as necessary and go to step h.

h. Check seating of Module. Should "bottom" against MDBP and latch should be flush against Front Panel assembly. If Module does not seat properly, return to factory.

i. Press **FILTER ON** softkey and check for flyers on waveform. If flyers observed, refer to paragraph 3-8. If no flyers observed, press FILTER OFF softkey. If flyers still not observed, consult factory. If flyers observed with filter off, replace INTF board (see paragraph 4-3.4 for removal, paragraph 7-1.2 for installation of replacement).

j. Perform delay calibration (see paragraph 3-18).

Level Error Correction

k. Repeat steps d. through j. If problems not solved, replace AMP assembly and ADC(A) board (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement pair).

l. Perform delay calibration again (see paragraph 3-18).

Gain Error Correction

m. Repeat steps d. through f. If problem(s) not solved, replace AMP assembly and ADC(A) board (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement pair).

n. Repeat step g. If problem(s) not solved, replace TMB board (see paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement).

o. Perform delay calibration again (see paragraph 3-18).

TDC Error Correction

p. Repeat steps d. through j. If problem(s) not solved, replace TMB board again.

q. Perform delay calibration again (see paragraph 3-18).

Trigger Error Correction

r. Repeat steps d. through f. If problem(s) not solved, replace TMB board again. If problem(s) solved, go to step s.

s. Repeat step g. If problem(s) not solved, replace AMP assembly and ADC(A) board again (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement pair).

t. Perform delay calibration again (see paragraph 3-18).

3-4. SYMPTOM: CHANNEL 1 OR 2 OR BOTH WILL NOT TRIGGER

DESCRIPTION:

When CH1 or CH2 trigger source selected, **NO OR SLOW TRIGGER** message displayed.

POSSIBLE FAULTS:

1. Defective AMP assembly
2. Defective ADC(A) board
3. Defective TMB board

REPAIR STEPS:

a. Select auto mode to apply slow software trigger and verify trigger level on affected channel(s). If both channels fail to trigger, replace TMB board (see paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement). If one channel triggers but not other, replace AMP assembly and ADC(A) board (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacements). If one channel still fails to trigger, replace TMB board again. If triggering problem remains, consult factory.

b. If replacement of defective AMP assembly or TMB or ADC(A) boards solves problem, perform delay calibration (see paragraph 3-18)

c. Perform system test (see paragraph 2-13).

3-5. SYMPTOM: ERROR DETERMINING MODULE TYPE

DESCRIPTION:

System passes turn-on test (see section 2) but **ERROR DETERMINING MODULE TYPE** message displayed during initialization (see figure 3-4).

POSSIBLE FAULTS:

1. Module seating problem
2. Module operating voltage(s) incorrect
3. INTF board read/write problems
4. INTF board EEPROM corrupted

REPAIR STEPS:

a. Check seating of Module. Should "bottom" against MDBP and latch should be flush against Front Panel assembly. If Module does not seat properly, return to factory.

b. Check voltage levels at ICON assembly connectors (see figure 3-5). If any voltage incorrect, check power sources in 7200 Mainframe (see figure 3-6). If any voltage in 7200 Mainframe incorrect, refer to LeCRoy 7000 series service manual for corrective action.

c. Check fuse F1 on TMB board (see figure B-4). If fuse open, replace TMB board (see paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement).

d. To generate Module identification information, reprogram EEPROM on INTF board by performing system test, selecting INTF as subassembly (paragraph 2-13, step c.), and selecting EEPRINTF as test to run (paragraph 2-13, step d.). When **Execute** softkey pressed, **TESTING EEPROM** message displayed.

   If Module identification not found, **THE MODULE ID WAS NOT PROGRAMMED TO 72XX, PROGRAMMING...** message displayed, followed by **RESTORING EEPROM, PLEASE WAIT** message. If error occurs, replace INTF board (see paragraph 4-3.4 for removal, paragraph 7-1.2 for installation of replacement).

e. If Module identification information obtained from EEPROM, both messages in step d. will be displayed, followed by **SERIAL NUMBER:** and **REVISION:0** messages. **SERIAL NUMBER:** message will not display serial number. If error occurs, replace INTF board again .

f. Press **Return** softkey to end test.

g. Perform delay calibration (see paragraph 3-18).

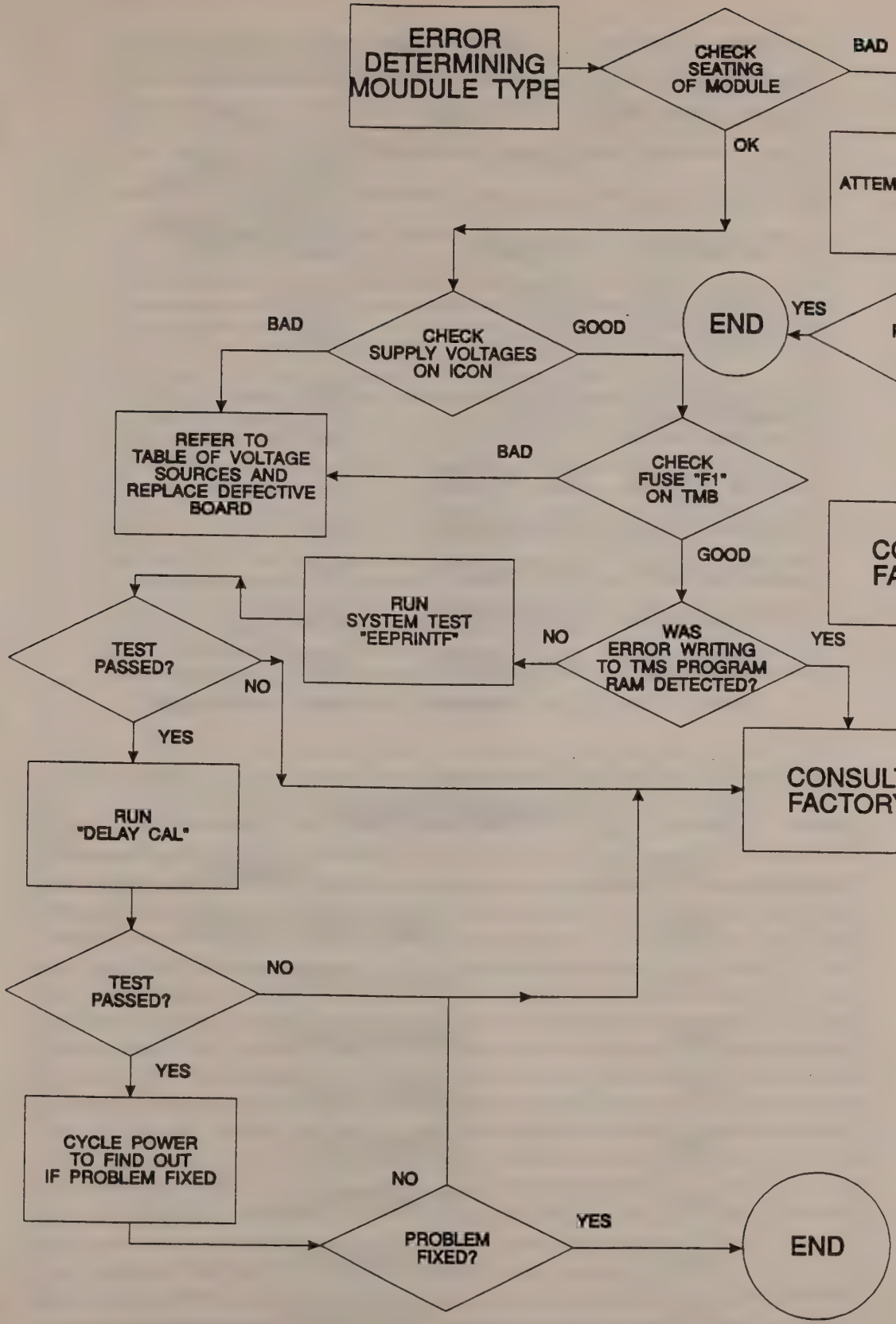


Figure 3-4. Error Determining Module Type Flow Diagram

ICON POWER SUPPLIES		
ICON CONNECTOR	PINS	SUPPLY
J12	A1, B1, C1	+24V BEFORE THERMAL SWITCH
J11, J12, J13, J14	A2, BS, C2	+24V AFTER THERMAL SWITCH
J11, J12, J13, J14	A3, B3, C3	+24V RETURN
J11, J12, J13, J14	A(4-7)	+5.1V
J11, J12, J13, J14	B(4-7)	+5.1V
J11, J12, J13, J14	C(4-7)	+5.1V
J11, J12, J13, J14	A(8-11)	-5.2V
J11, J12, J13, J14	B(8-11)	-5.2V
J11, J12, J13, J14	C(8-11)	-5.2V
J11, J12, J13, J14	A12, B12, C12	-2V
J11, J12, J13, J14	A13, B13, C13	+8V
J11, J12, J13, J14	A14, B14, C14	-8V
J11, J12, J13, J14	A15. B15. C15	+15V
J11, J12, J13, J14	A16, B16, C16	-15V

Figure 3-5. ICON Assembly Voltage Checkpoints

ICON POWER SUPPLIES	
SUPPLY	SOURCE
+24V	7200 POWER SUPPLY
+5.1V	MEM (DC/DC)
-5.2V	ADC (DC/DC)
-2V	MEM (DC/DC)
+8V	TMB (DC/DC)
-8V	TMB (DC/DC)
+15V	TMB (DC/DC)
-15V	TMB (DC/DC)

Figure 3-6. ICON Assembly Power Sources

h. Turn 7200 Mainframe off, then restart. If error occurs, replace INTF board again.

i. Perform system test (paragraph 2-13).

3-6 SYMPTOM: EXCESSIVE NOISE

DESCRIPTION:

Waveforms on CH1 and CH2 or both exhibit excessive noise.

POSSIBLE FAULTS:

1. 7200 Mainframe power supplies
2. Defective AMP assembly
3. Defective ADC(A) board
4. Defective TMB board

REPAIR STEPS:

a. Refer to flow diagram, figure 3-7. Perform baseline noise test (see paragraph 2-4) to determine whether noise due to power supply oscillation, flyers (spike noise), defective AMP assembly, or defective ADC(A) board. If noise due to power supply oscillation, check ICON assembly voltages (figure 3-5). If voltage(s) incorrect, check voltage sources in 7200 Mainframe (see figure 3-6), then refer to LeCroy 7000 series service manual for corrective action. If noise due to flyers, refer to paragraph 3-8. If noise due to defective AMP assembly, refer to paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement. If noise due to defective TMB board, refer to paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement.

b. Repeat step a. If excessive noise still present, replace TMB board again.

c. Perform delay calibration in accordance with paragraph 3-18.

d. Perform system test (paragraph 2-13).

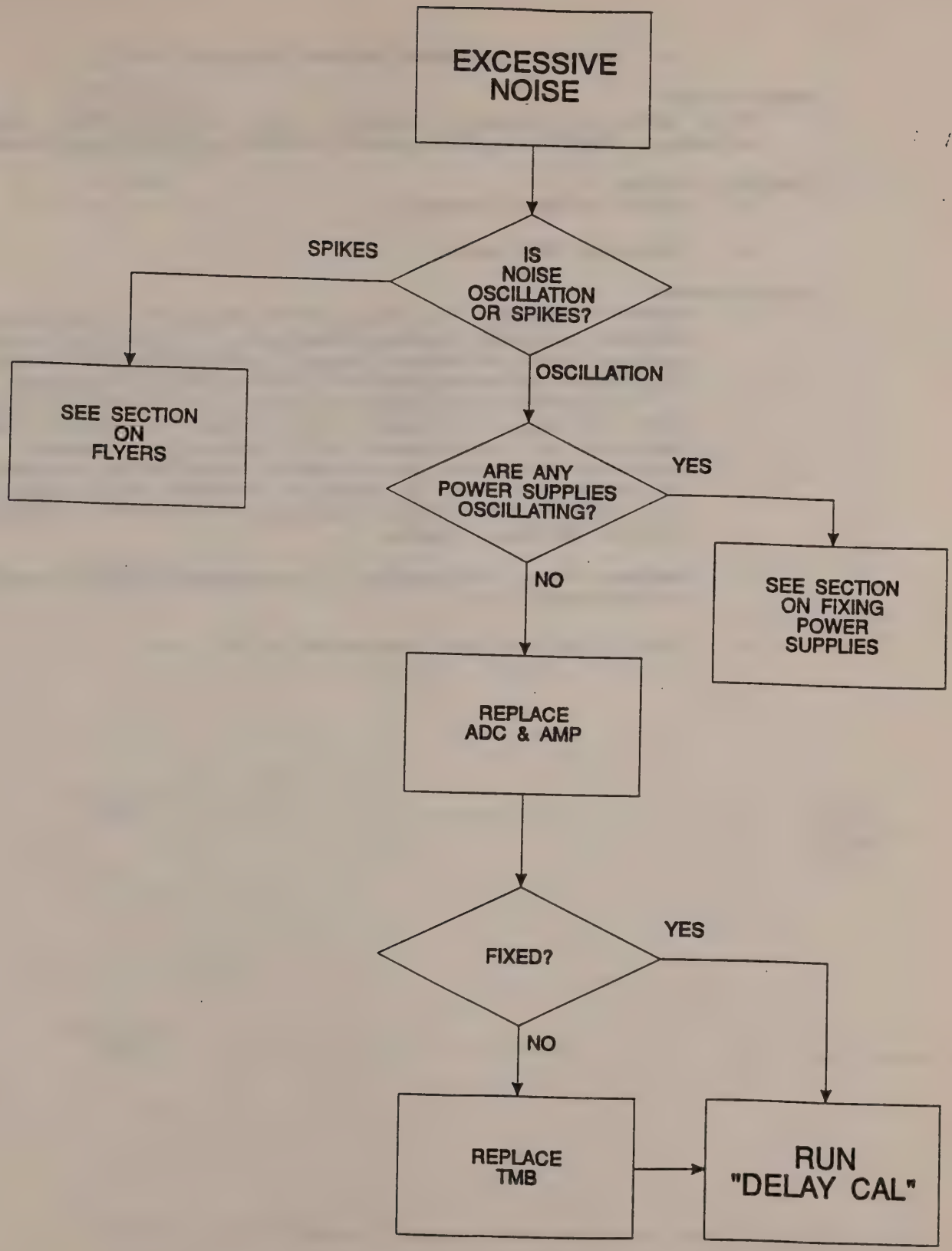


Figure 3-7. Excessive Noise Flow Diagram

3-7 SYMPTOM: EXTERNAL TRIGGER DOES NOT WORK

DESCRIPTION:

When external trigger selected and valid trigger level selected, PLUG-IN X: NO OR SLOW TRIGGERS message displayed

POSSIBLE FAULTS:

1. Defective EXTR assembly
2. Defective TMB board

REPAIR STEPS:

a. Refer to figure 3-8. Check both channels to determine whether external trigger functions. If external trigger does not work on either channel 1 or channel 2, replace TMB board (see paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement). If external trigger does not work on channel 1 or channel 2, replace EXTR assembly in accordance with removal procedure in paragraph 4-3.1 and new assembly installation procedure in paragraph 7-1.5. If external trigger still works on only one channel after replacement of EXTR assembly, replace TMB board again.

b. Perform delay calibration in accordance with procedure in paragraph 3-18.

c. Perform system test (paragraph 2-13).

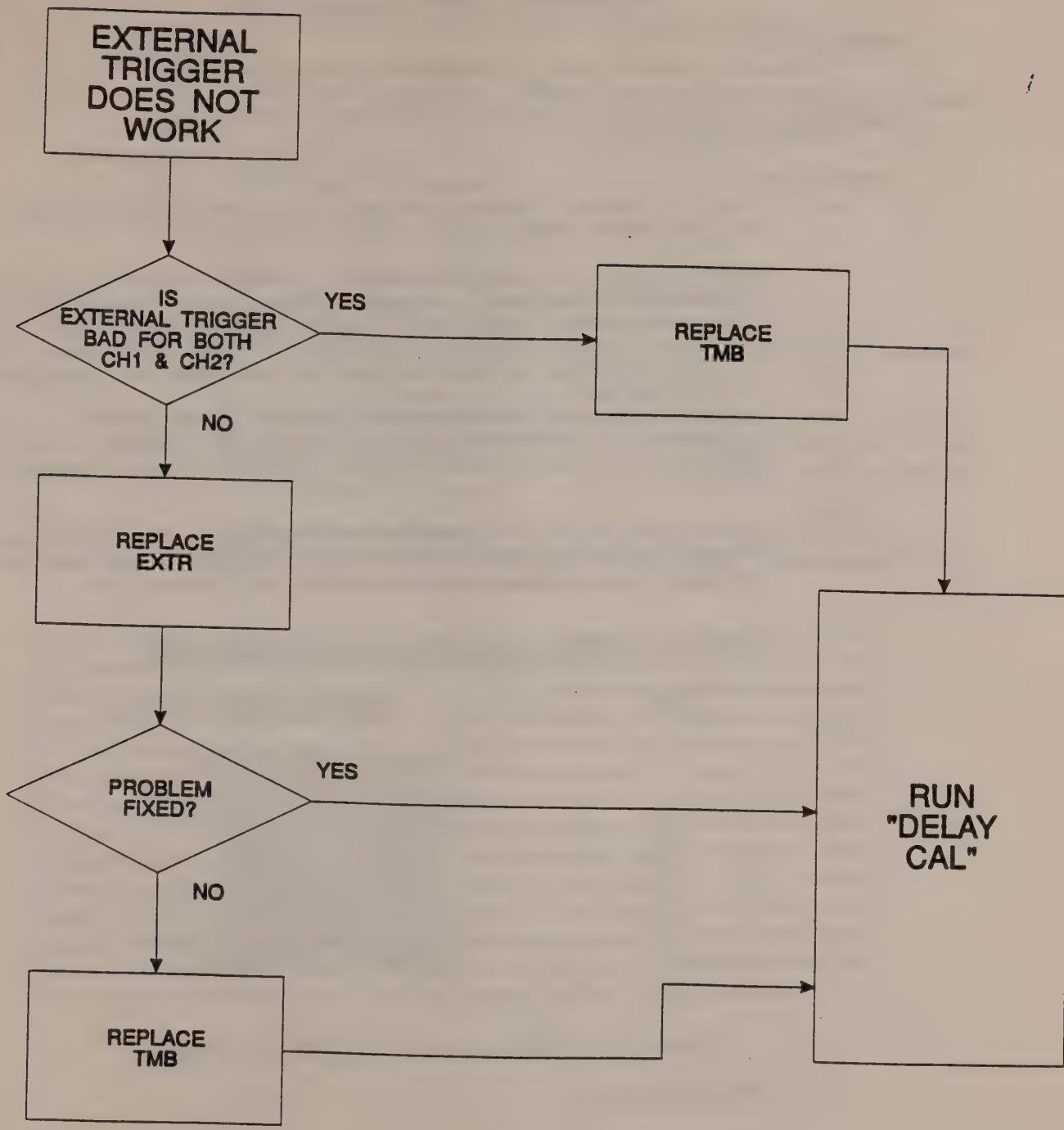


Figure 3-8. External Trigger Does Not Work Flow Diagram

3-8 SYMPTOM: FLYERS (SPIKE NOISE)

DESCRIPTION:
Transient distortion of observed waveforms

POSSIBLE FAULT:
Timing Problems

REPAIR STEPS:

a. Turn off power. Connect dongle to Centronics port on Rear of 7200 Mainframe.

b. Apply power to 7200 Mainframe. Press MODIFY key and INTERLEAVED SAMPLING softkey on Front Panel assembly of 7200 Mainframe. Press CAL CLK ON softkey and check for display of 15.56 MHZ square wave without flyers. If flyers observed, press CAL CLK OFF softkey and TURN OFF FILTER softkey. Go to step c.

c. On ADC(A) board, mark original position of VARDLY 4 and 5 wipers (see figure B-3 for location of VARDLY 4 and 5) and rotate wipers 3-4 clicks cw or ccw to eliminate flyers.

d. Erase system log. If problem not solved, move offset and observe waveform for flyers at bit switching points. For vertical resolution per bit, refer to figure 3-9.

VERTICAL RESOLUTION PER BIT IS AS FOLLOWS	
BIT	VERTICAL RESOLUTION
0	1/32 MAJOR DIVISION
1	1/16 MAJOR DIVISION
2	1/8 MAJOR DIVISION
3	1/4 MAJOR DIVISION
4	1/2 MAJOR DIVISION
5	1 MAJOR DIVISION
6	2 MAJOR DIVISIONS
7	4 MAJOR DIVISIONS

Figure 3-9. Vertical Resolution Per Bit

e. Repeat step c.

3-9 SYMPTOM: GAIN ERRORS OR GAIN INCORRECT

DESCRIPTION:

During self-calibration, **DYNAMIC CALIBRATION FAILURE** message displayed or multiple gain errors entered into system log

POSSIBLE FAULTS:

1. Defective TMB board
2. Defective AMP assembly
3. Defective ADC(A) board

REPAIR STEPS:

a. Refer to figure 3-10 and system log to determine whether CH1, CH2, or both affected.

b. If **both** channels affected, replace TMB board by removing in accordance with procedure in paragraph 4-3.3 and installing replacement board in accordance with procedure in paragraph 7-1.3.

c. If **one** channel affected, replace AMP assembly and ADC(A) board (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement pair).

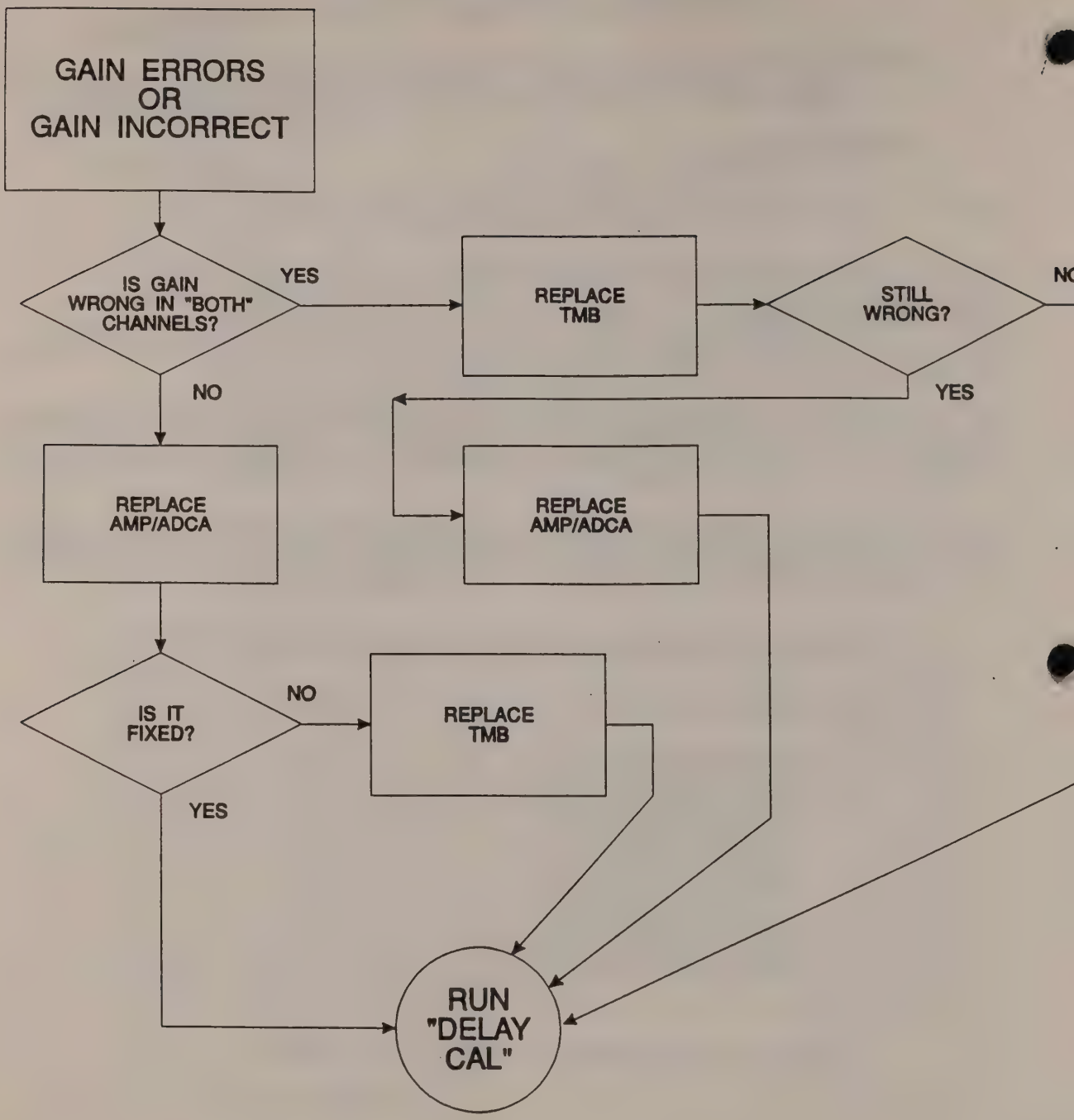


Figure 3-10. Gain Errors or Gain Incorrect Flow Diagram

d. Clear system log and force several calibration cycles by switching voltage ranges or by running allcal routine.

NOTE

The ALLCAL program forces the 7200 Mainframe to perform self-calibration repeatedly. It is particularly useful for overnight or extended testing to detect calibration errors.

The program should be allowed to run long enough to genersate a statistically significant summary of good and bad calibration cycles. Every few seconds, a calibration cycle will be completed and the good and bad calibration tally displayed will be updated.

Whenever a calibration cycle is complete and the dispay updated, the program changes acquisition parameters (input coupling, BWL on/off, input range, etc.). Every possible configuration is tested after every 150 calibration cycles.

All Plug-In Modules will have some bad calibration cycles which will be recorded in the system log. Excessive errors of the same type indicate that repair is necessary.

To perform the allcal routine, use the following procedure:

(1) Insert "allcal" diskette in floppy disk drive of 7200 Mainframe.

(2) Erase system log.

(3) Recall and run "allcal" program

(4) Allow "allcal" program to execute at least 1000 calibration cycles unless bad calibration rate is very high

(5) Record number of good and bad calibration cycles

(6) Inspect system log (see figure 3-11) for calibration errors. If problem remains unresolved, consult factory.

(7) Perform system test (paragraph 2-13)

```
00800000 TDC CAL NO POSITIVE EDGE
01000000 TDC CAL NO TRANSITION
02000000 TDC CAL SMALL RANGE
04000000 TRIG LEVEL CAL ERROR
08000000 TRIG GAIN CAL ERROR
```

Figure 3-11. Logged Calibration Errors

3-10 SYMPTOM: NO SIGNAL, TRACE OFF SCREEN

DESCRIPTION:

Traces for one or both input channels cannot be displayed, even with input open and offset set to 0. Trace indicated as off screen by up or down arrows at edge.

POSSIBLE FAULTS:

1. Defective ADC(A) board
2. Defective AMP Assembly
3. Defective MEM(A) board
4. Defective TMB board

REPAIR STEPS:

a. Refer to figure 3-12. Check ICON assembly for voltages listed in figure 3-5. If any voltage is missing or incorrect, check ICON assembly voltage sources listed in figure 3-6. Troubleshoot and repair power supply in 7200 Mainframe by referring to LeCroy 7000 series repair manual for corrective action.

b. If all voltages present, turn on calibration clock (paragraph 3-20) and check for display of 15.56 MHZ square wave. If square wave displayed, go to step f.

c. If square wave not displayed, perform memory test portion of system test (paragraph 2-13). If memory test passed, replace AMP assembly and ADC(A) board (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement pair). If memory test failed, replace MEM(A) board, following procedure in paragraph 4-3.5 for removal and procedure in paragraph 7-1.1 for installation of replacement. If problem corrected, go to step f.

d. Determine whether baseline is offscreen in both 1 megohm and 50 ohm operating modes. If trace not off screen in both modes, replace AMP assembly and ADC(A) board again. If problem resolved, go to step f., otherwise go to step e.

e. Determine whether baseline is off screen for both channels. If trace not offscreen, replace AMP assembly-ADC(A) board pair again.

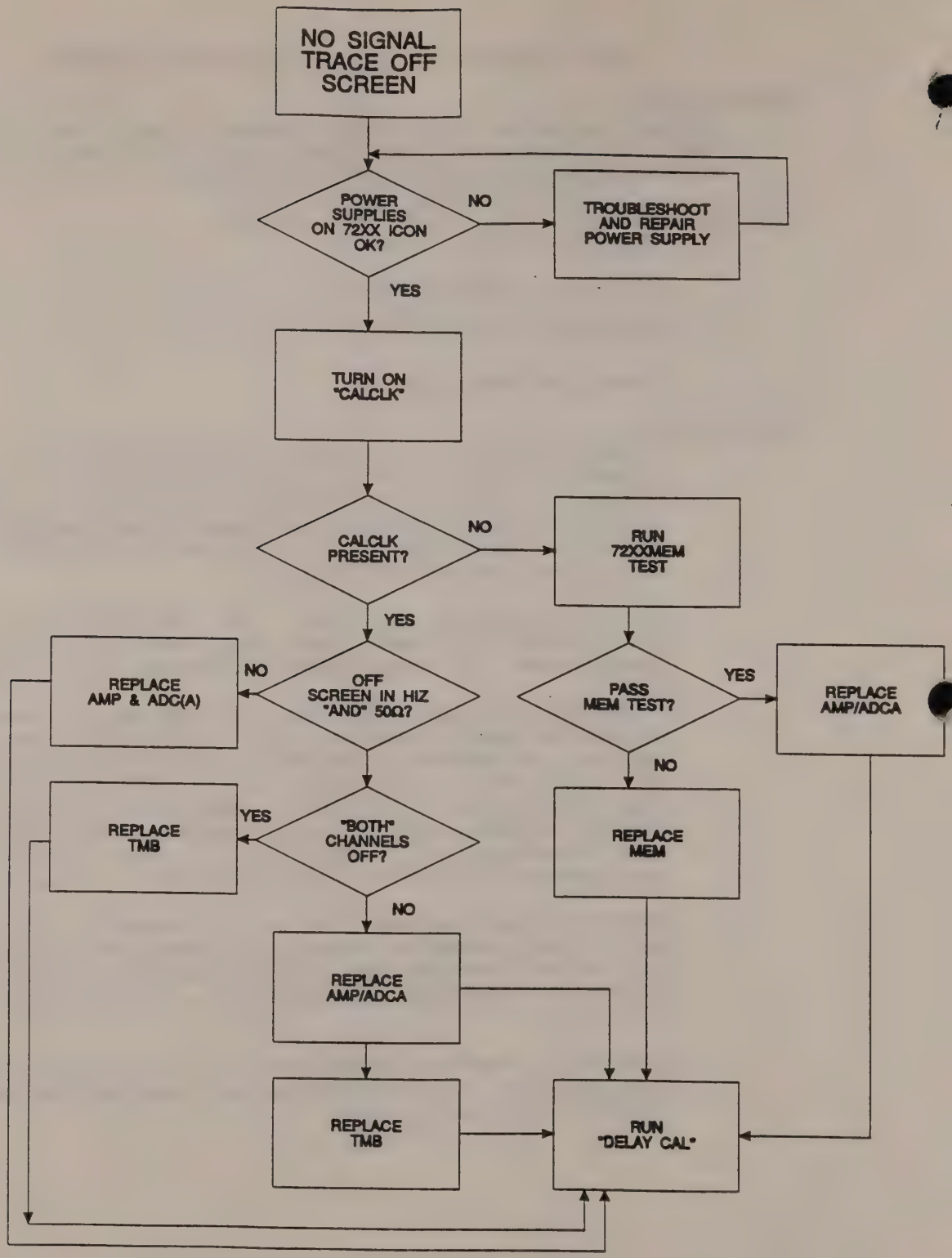


Figure 3-12. No Signal, Trace Off Screen Flow Diagram

If trace still offscreen, replace TMB board (see paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement.

f. Perform delay calibration in accordance with procedure in paragraph 3-18.

g. Retest.

3-11 SYMPTOM: OFFSET DRIFTS

DESCRIPTION:

Noticeable offset drift with signal applied at stable dc level or baseline drift with no signal applied. Drift noticeable even after 7200 Mainframe powered up for several minutes and has had sufficient time for thermal stabilization

POSSIBLE FAULTS:

1. Drift in 7200 Mainframe power supply
2. Defective ADC(A) board
3. Defective AMP assembly
4. Defective TMB board

REPAIR STEPS:

a. Refer to figure 3-13. Determine whether offset drift occurs in both channels. If both channels drifting, check ICON assembly voltage inputs listed in figure 3-5 for oscillation. If oscillation detected, check ICON assembly voltage sources listed in figure 3-6 for oscillation. Troubleshoot and repair power supply in 7200 Mainframe by referring to LeCroy 7000 series repair manual for corrective action. If problem solved, go to step d.

b. Turn on calibration clock (paragraph 3-8, step b.) and determine whether 15.56 MHZ square wave drifts in the same direction as output. If so, replace AMP assembly and ADC(A) board in accordance with removal procedure in paragraph 4-3.2 and installation procedure in paragraph 7-1.4. If not, replace TMB board (see paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement) and go to step c.

c. Check for signal drift. If still occurring, remove replacement TMB board and reinstall original TMB board. Replace AMP assembly and ADC(A) board again. If problem solved, go to step d. If not, consult factory.

d. Perform delay calibration (paragraph 3-18).

e. Retest.

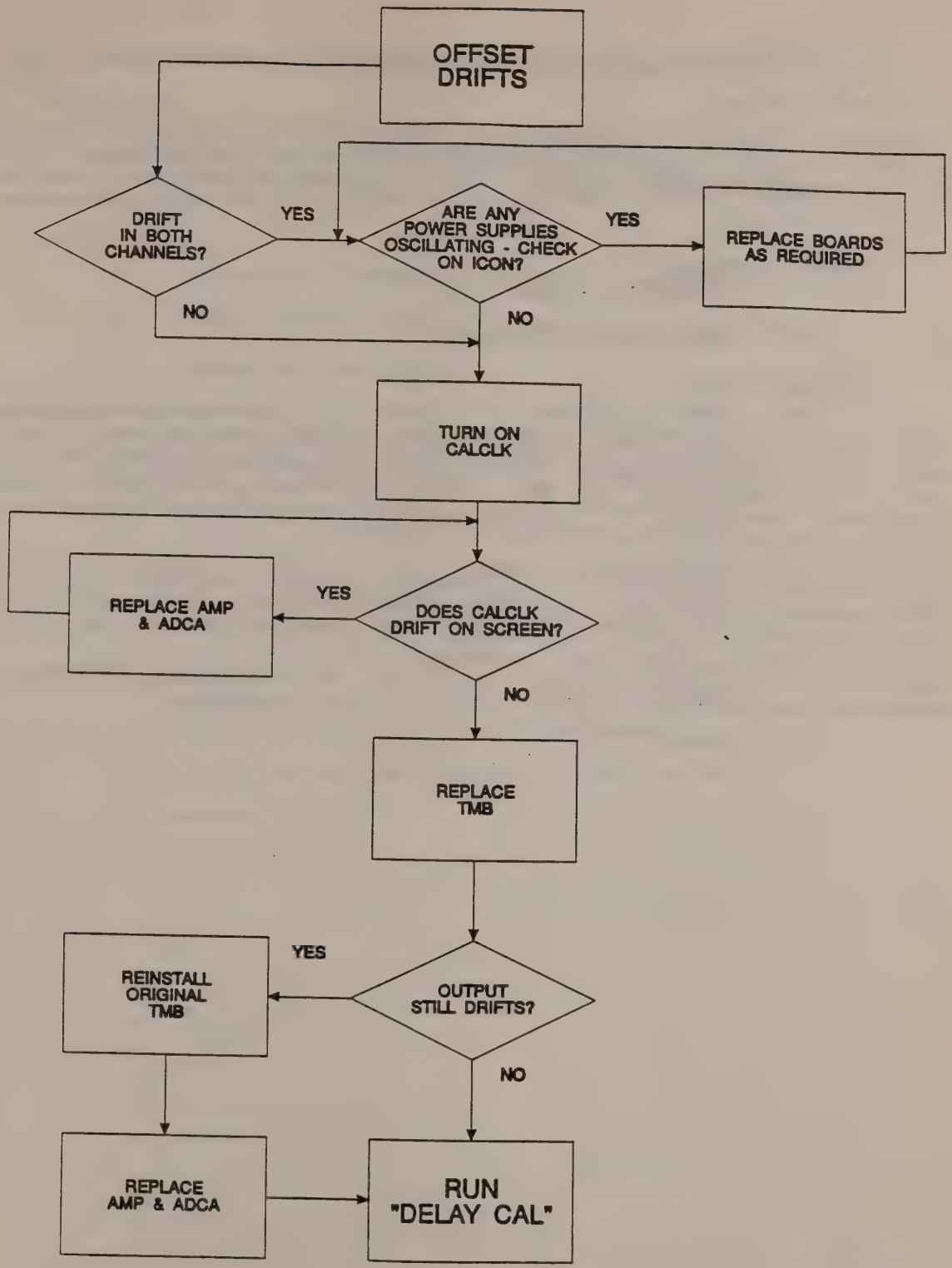


Figure 3-13. Offset Drifts Flow Diagram

3-12 SYMPTOM: PLUG-IN NOT INITIALIZED, NO FRONT PANEL LIGHTS

DESCRIPTION:

7200 Mainframe power-on initialization procedure does not result in display of Plug-In Module as connected device even though Plug-In Module is installed and properly seated in MFMB. Plug-In Module has no indicators active and appears to be dead.

POSSIBLE FAULTS:

1. Missing voltages

2. Defective INTF board

REPAIR STEPS:

a. Refer to figure 3-5. Check ICON assembly voltage inputs. If oscillation detected, check ICON assembly voltage sources listed in figure 3-6. Troubleshoot and repair power supply in 7200 Mainframe by referring to LeCroy 7000 series repair manual for corrective action. If problem solved, go to step c.

b. Check fuses on INTF board (see figure B-5 for locations). If fuses not blown, consult factory. If fuses blown and replacement does not solve problem, consult factory.

c. Perform delay calibration by following procedure in paragraph 3-18.

d. Retest.

3-13 SYMPTOM: PROBE ATTENUATION CHANGES INTERMITTENTLY

DESCRIPTION:

Vertical scale changes intermittently. Probe attenuation status settings alternate between x1 and x10. RCL program execution may be interrupted. **PROBE MISMATCH** message may be displayed.

POSSIBLE FAULTS:

1. Front Panel assembly improperly assembled

2. Defective probe rings or probe ring insulators

3. Defective INTF board

REPAIR STEPS:

a. Refer to figure 3-14. Measure 5 VDC level on probe rings for stability. If stable, replace INTF board (see paragraph 4-3.4 for removal, paragraph 7-1.2 for installation of replacement). If 5 VDC level unstable, inspect insulation around probe ring to be sure of isolation from Front Panel assembly which is at ground level. Adjust assembly or repair insulation. If insulation cannot be repaired, replace AMP assembly-ADC board pair or EXTR assembly as necessary. See paragraph 4-3.2 for AMP assembly and ADC(A) board removal, paragraph 7-1.4 for installation of replacement pair. See paragraph 4-3.1 for EXTR assembly removal and paragraph 7-1.5 for installation of replacement.

b. Perform delay calibration (paragraph 3-18).

c. Retest

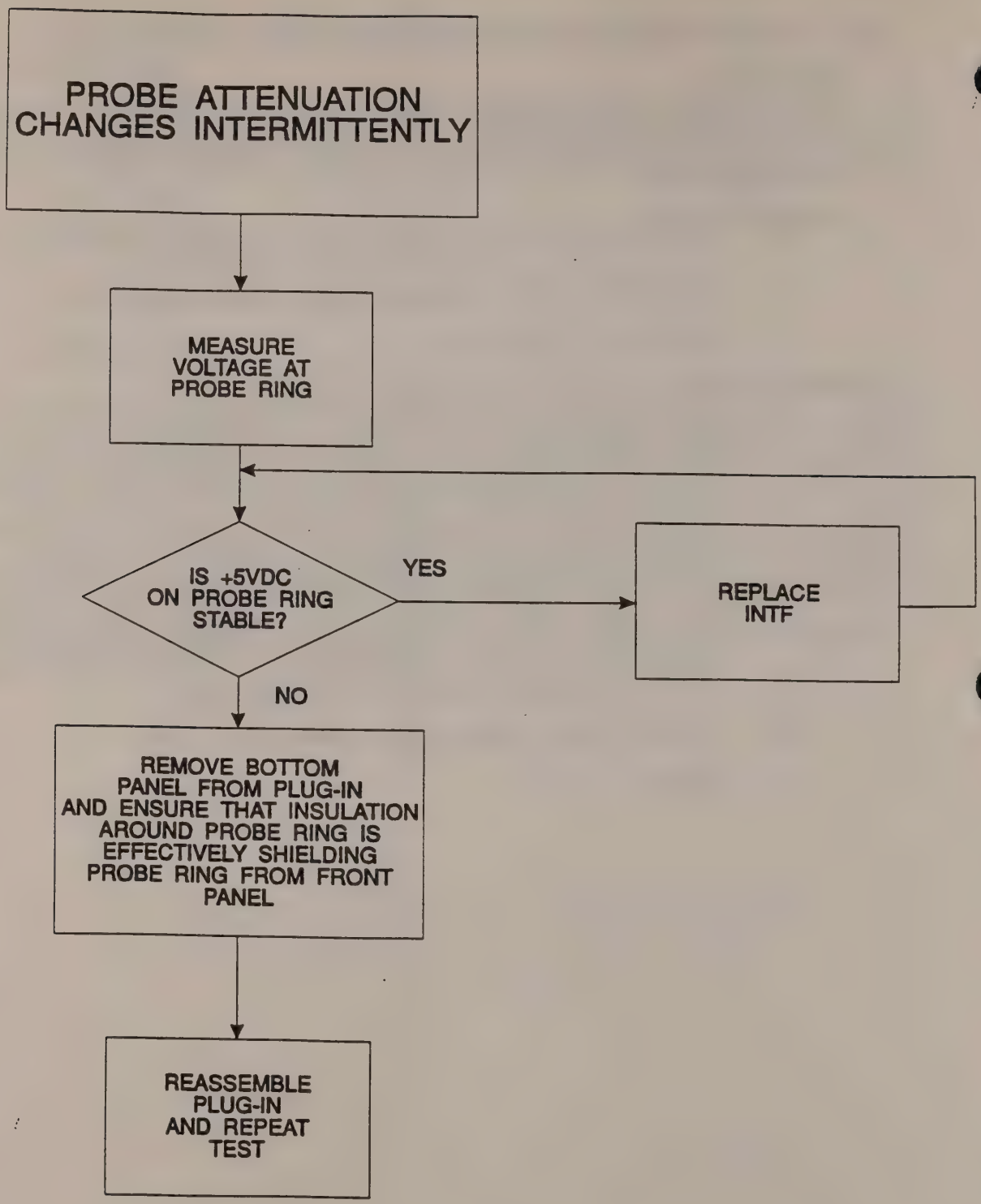

PROBE ATTENUATION CHANGES INTERMITTENTLY
MEASURE VOLTAGE AT PROBE RING
IS +5VDC ON PROBE RING STABLE?
YES
REPLACE INTF
NO
REMOVE BOTTOM PANEL FROM PLUG-IN AND ENSURE THAT INSULATION AROUND PROBE RING IS EFFECTIVELY SHIELDING PROBE RING FROM FRONT PANEL
REASSEMBLE PLUG-IN AND REPEAT TEST

Figure 3-14. Probe Attenuation Changes Intermittently Flow Diagram

3-14 SYMPTOM: STUCK IN CALIBRATION MODE

DESCRIPTION:

Calibration icon in lower left corner of display comes on and stays on

POSSIBLE FAULTS:

1. Power supply voltages missing or incorrect
2. Defective ADC(A) board
3. Defective TMB board
4. Defective MEM(A) board
5. Defective EXTR assembly
6. Defective AMP assembly
7. Defective INTF board

REPAIR STEPS:

a. Refer to figure 3-5. Check ICON assembly voltage inputs. Check ICON assembly voltage sources listed in figure 3-6. Troubleshoot and repair power supply in 7200 Mainframe by referring to LeCroy 7000 series service manual for corrective action.

b. Refer to figure 3-15. Check for ADC clock pulses on pins A28 and A29 of J33. If pulses missing, go to step c. If pulses present, go to step d.

c. Check for logic 0 level on pin A31 of J34. If level not 0, replace TMB board by removing in accordance with procedure in paragraph 4-3.3 and installing replacement in accordance with procedure in paragraph 7-1.3. If level still not 0, replace INTF board (see paragraph 4-3.4 for removal, paragraph 7-1.2 for installation of replacement). If problem remains, consult factory. If problem corrected, replace AMP assembly-ADC(A) board pair, following procedure in paragraph 4-3.2 for removal and procedure in paragraph 7-1.4 for installation of replacement pair and go to step f.

d. Perform system test (see paragraph 2-13), selecting TMB as subassembly to test and TEST_TMB as test to run. Press **Execute** softkey, then **Yes** softkey twice. If **PASSED** displayed, problem solved. If not, go to step e.

e. Check pin A44 of J33 on ICON assembly for pulsing. If pulses not detected, remove AMP and EXTR assemblies and repeat step d. If pulses still not detected, replace TMB board (see paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement) and go to step f. If pulses detected, reinstall AMP assembly and repeat step d.

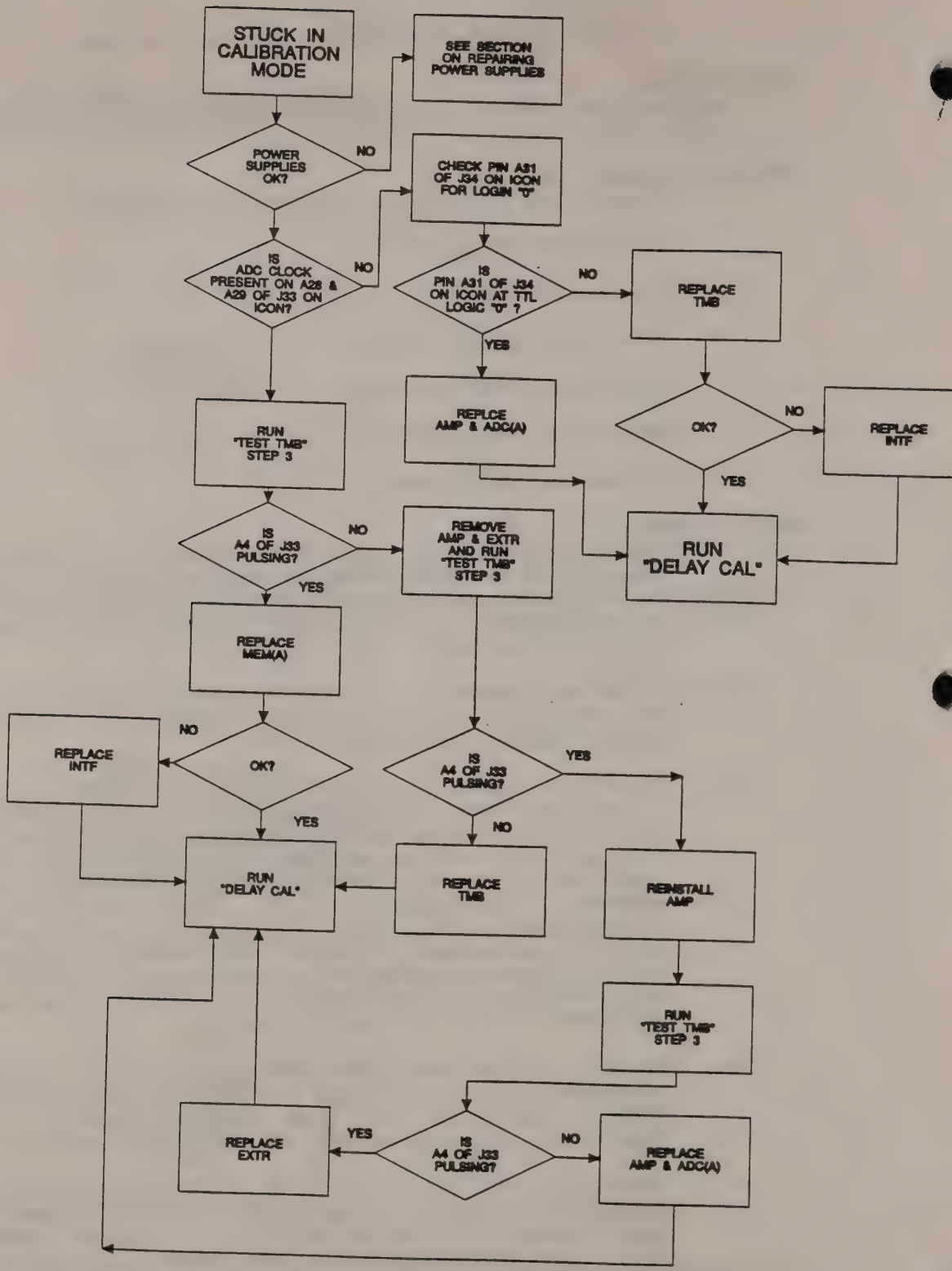


Figure 3-15. Stuck in Calibration Mode Flow Diagram

If, after reinstalling AMP assembly, pulses not detected replace AMP assembly and ADC(A) board again and repeat step d. If pulses detected, replace EXTR assembly by following procedure in paragraph 4-3.1 for removal and procedure in paragraph 7-1.5 for installation of replacement. If problem not solved, consult factory. If problem solved, replace MEM(A) board (see paragraph 4-3.5 for removal, paragraph 7-1.1 for installation of replacement) and go to step f. If not, replace INTF board again. If problem solved, go to step f. If not, consult factory.

f. Perform delay calibration, following procedure in paragraph 3-18.

g. Retest.

3-15 SYMPTOM: TIMEBASE IS WRONG

DESCRIPTION:

Input signal of known frequency displayed incorrectly (wrong frequency)

POSSIBLE FAULTS:

1. Defective ADC(A) board

2. Defective TMB board

REPAIR STEPS:

a. If **TIMEBASE PHASE UNLOCKED** message also displayed, refer to paragraph 3-16, TIMEBASE PHASE UNLOCKED.

b. At front of 7200 Mainframe, rotate **Move Box** knob to select Max Memory size of 20K as shown in figure 3-16.

c. Set **A:TIMEBASE** to 2 us/div. Steps b. and c. force Plug-In Module to operate in four flash mode. A sine wave input was used to produce figure 3-14, showing grid divided into four parts. From left to right, flash ADCs D,C,B, and A occupy 2-1/2 divisions apiece.

d. Inside Module, find connector J5 on ADC(A) board (see figure B-3 for location) and verify presence of 250 MHZ sample clock signal. If signal present, replace TMB board by removing in accordance with procedure in paragraph 4-3.3 and installing replacement in accordance with procedure in paragraph 7-1.3. If 250 MHZ signal not present, replace AMP assembly-ADC(A) pair (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement pair.

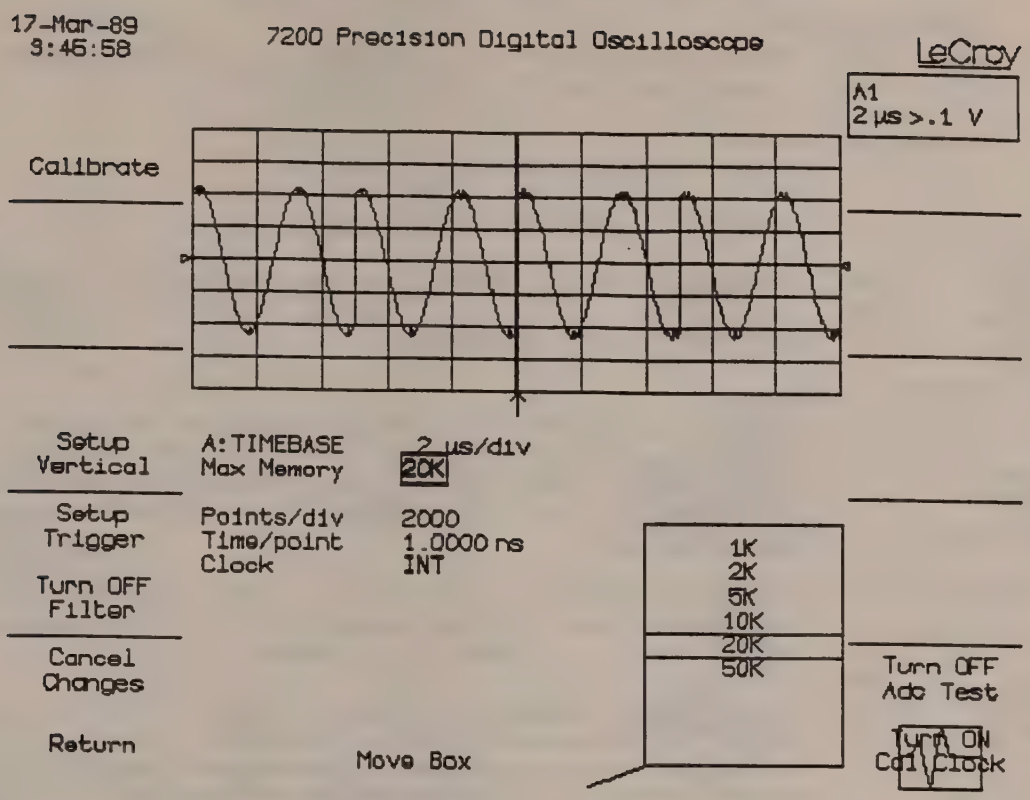


Figure 3-16. ADC Test Display

e. Perform delay calibration (see paragraph 3-18).

f. Retest.

3-16. SYMPTOM: **TIMEBASE PHASE UNLOCKED** MESSAGE DISPLAYED OR LOGGED

DESCRIPTION:

Same as for symptom 3-15. If logged but not displayed, may be due to poor seating of Plug-In Module.

POSSIBLE FAULTS:

1. Plug-In Module seating problem
2. Missing 10 MHZ reference clock pulses
3. Defective ADC(A) board (clock problem)
4. MEM board cable problem

REPAIR STEPS:

a. Refer to figure 3-17. Check seating of Module. Should "bottom" against MDBP and latch should be flush against Front Panel assembly. If Module does not seat properly, return to factory. If MOdule properly seated, go to step b.

b. Determine whether system is "hung in calibration" (CAL indicator comes on and stays on). If CAL indicator on, go to step c. If not, go to step e.

c. Check ICON assembly voltage inputs (see figure 3-5). Check ICON assembly voltage sources listed in figure 3-6. Troubleshoot and repair power supply in 7200 Mainframe by referring to LeCroy 7000 series repair manual for corrective action. If problem solved, go to step j. If not, go to step d.

d. Check for presence of ECL clock pulses on pins A27 and A28 of connector J33 on ICON assembly. If clock pulses present, replace TMB board (see paragraph 4-3.3 for removal, paragraph 7-1.3 for installation of replacement). If problem solved, go to step j. If not, consult factory. If clock pulses not present, replace AMP assembly-AC(A) card pair, following procedure in paragraph 4-3.2 for removal and procedure in paragraph 7-1.4 for installation of replacement pair.

e. At front of 7200 Mainframe, rotate Move Box knob to select Max Memory size of 20K as shown in figure 3-14.

f. Set A:TIMEBASE to 2 us/div. Steps e. and f. force Plug-In Module to operate in four flash mode.

g. Press **CAL CLK** softswitch and use cursor measurements on 7200 Mainframe to determine frequency. If nominal frequency 15 MHZ, consult factory. If frequency not 15 MHZ, go to step h.

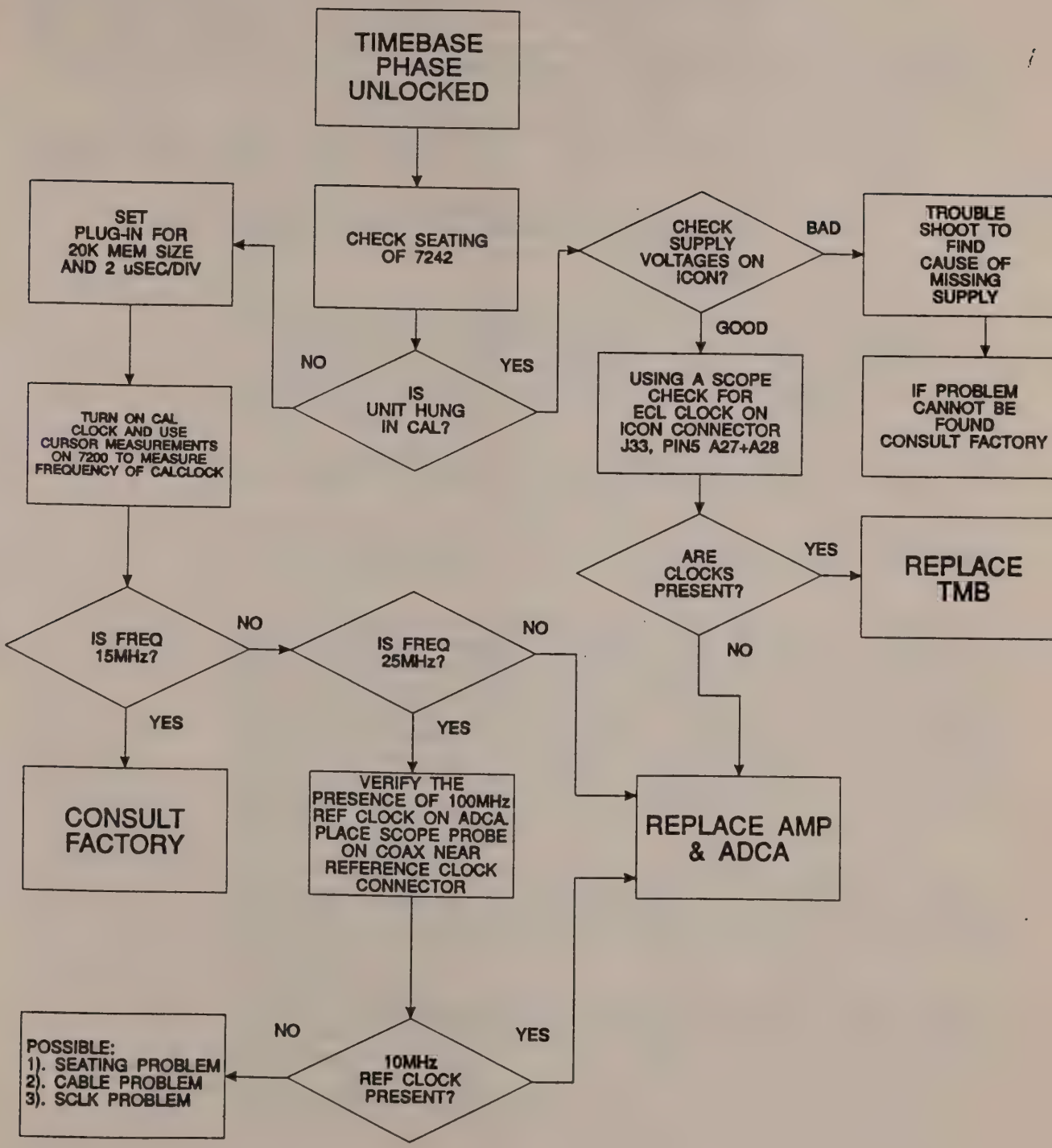


Figure 3-17. Timebase Phase Unlocked Flow Diagram

h. If nominal CAL CLK frequency 25 MHZ, verify presence of 10 MHZ reference clock pulses on ADC(A) board by placing scop[e probe on coax cable near connector. If 10 MHZ pulses not present, replace AMP assembly-ADC(A) board pair again. If problem not corrected, consult factory. If problem corrected, go to step j.

i. Recheck Module seating and verify proper connection of all signal cables. If problem still not solved, consult factory.

j. Perform delay calibration (see paragraph 3-18).

k. Retest.

3-17 SYMPTOM: TRIGGER DELAY PROBLEMS

DESCRIPTION:

Trigger delay not within specifications for Plug-In Module.

POSSIBLE FAULTS:

1. Delay calibration not performed
2. Defective TMB board
3. Defective AMP assembly
4. Defective ADC(A) board

REPAIR STEPS:

a. Perform delay calibration (paragraph 3-18). If successful no further action required. If delay calibration unsuccessful, rotate **Move Box** knob at front of 7200 Mainframe to select Max Memory size of 20K as shown in figure 3-16.

b. Set **A:TIMEBASE** to 2 us/div. Steps e. and f. force Plug-In Module to operate in four flash mode or 1 ns/point.

c. Measure frequency of ADC clock pulses on connector J5 of ADC(A) board (see figure B-3 for location). Frequency should be 250 MHZ.

d. Set **A:TIMEBASE** to 5us/div. ADC clock frequency should be 200 MHZ. If frequency correct, go to step e. If not, check for presence of 10 MHZ reference signal on ADC(A) board. If not present, check seating of Module. Should "bottom" against MDBP and latch should be flush against Front Panel assembly. If Module does not seat properly, return to factory. If 10 MHZ signal present, replace AMP assembly-ADC(A) board pair (see paragraph 4-3.2 for removal, paragraph 7-1.4 for installation of replacement pair).

e. Perform delay calibration again. Verify whether delay problems occur on all channels. If so, replace TMB board, following procedure in paragraph 4-3.3 for removal and procedure in paragraph 7-1.3 for installation of replacement.

f. Perform delay calibration again. If problem affects only one channel (CH1 or CH2), replace AMP assembly-ADC(A) board pair again.

g. Perform delay calibration again.

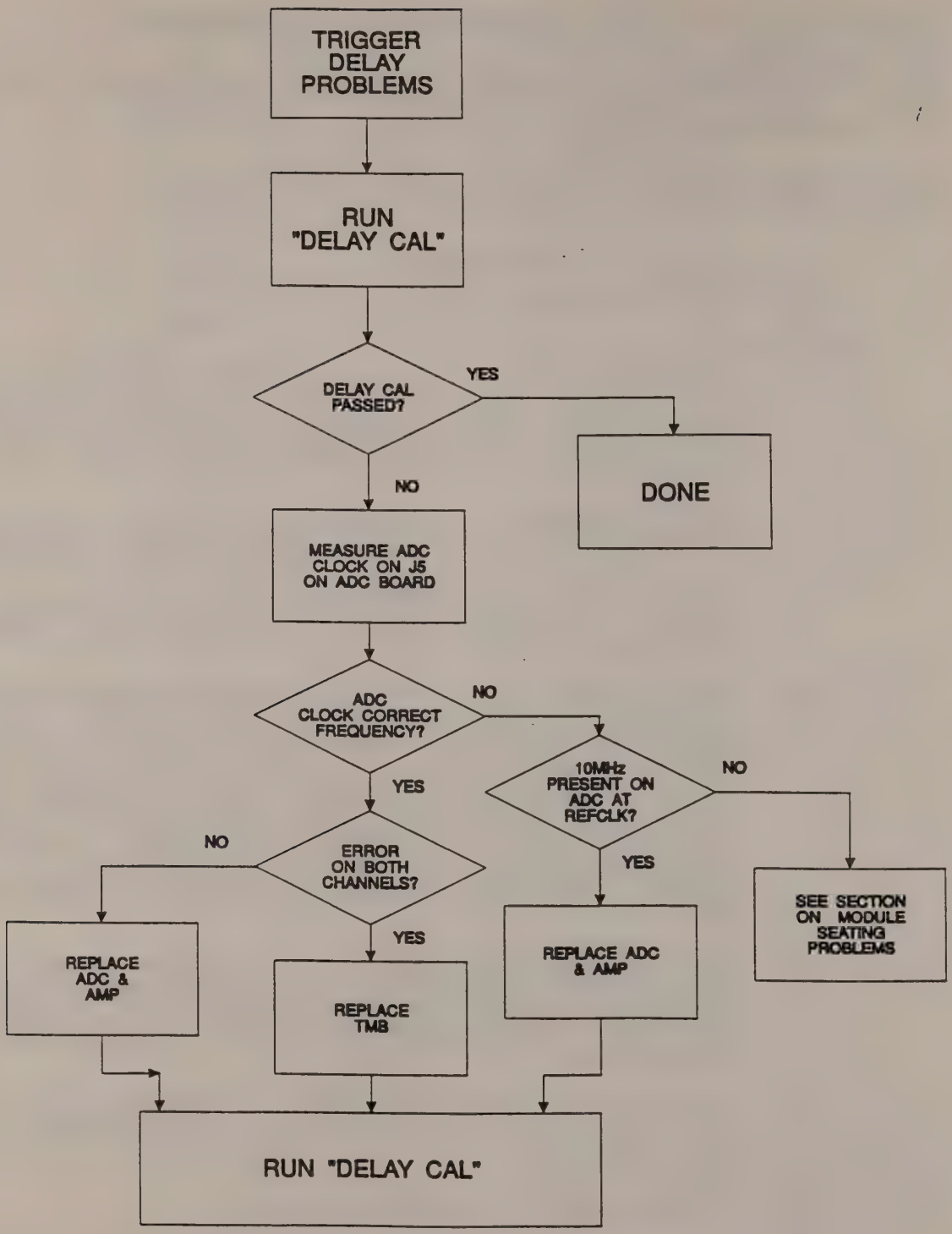


Figure 3-18. Trigger Delay Problems Flow Diagram

3-18 Delay Calibration

Delay calibration is performed whenever any assembly or board is adjusted, repaired, or replaced. The program calculates trigger delay error on the basis of statistical analysis (histograms) of the trigger location and stores correction coefficients in the EEPROM on the INTF board.

There are three versions of delay calibration (DELAY CAL) software. The correct version to use may be determined from the following:

VERSION	APPLICABILITY
1	Older Modules that have HTRs (serial numbers A85000 - A85550). Many of the Modules within this group have been retrofitted with PTRs, in which case version 2 should be used.
2	Modules with PTRs.
3	7242A Plug-In Modules.

To perform delay calibration, use the following procedure:

a. Attach dongle to Centronics port on Rear of Mainframe.

b. Insert correct version of delay calibration diskette in floppy drive.

c. Apply power to 7200 Mainframe. System should boot from floppy drive.

d. Respond to prompts displayed on CRT screen.

e. Apply 1 volt p-p, 5 KHz square wave to A1.

f. Press **Return** softkey to continue. After 1 to 2 minutes a **PASSED** or **FAILED** message will be displayed.

g. Remove calibration diskette from floppy drive and insert system test diskette. Perform bandwidth test (paragraph 2-9). If bandwidth test fails, consult factory.

SECTION 4 REMOVAL

4-1 Front Panel Assembly and Rail Assembly

To remove the front panel assembly and the rail assembly, use the following procedure:

a. Turn 7242 Plug-In Module upside down as shown in figure 4-1 and remove 4 short screws (item A) that attach front panel assembly to housing.

NOTE

For later reassembly, note that the housing fits inside the rail assembly. There are 2 screws on each side that attach the housing to the front panel, 2 screws on each side that attach the housing to the rail, and 2 screws that attach the rear bracket assembly to the rail assembly.

b. Remove 2 long flat Phillips head screws (item B) that attach rail assembly to amplifier .

c. Remove 2 long flat Phillips head screws (item B) that attach rail assembly to external trigger assembly.

d. At rear of 7242 Plug-In Module, remove 2 shorter flat Phillips head screws (item C) that attach rear bracket assembly to rail assembly.

e. Pull up rail assembly and remove to allow front panel assembly to be removed, then carefully pull front panel assembly out of housing, being careful to avoid damaging probe rings around CH1, CH2, and EXT TRIG connectors if present (in some models).

4-2 Rear Bracket Assembly

To remove the rear bracket assembly after the rail assembly and front panel assembly have been removed, use the following procedure:

a. Remove 2 flat Phillips head screws which attach rear bracket assembly to housing, then pull rear bracket assembly out and away from housing to remove.

b. Remove housing.

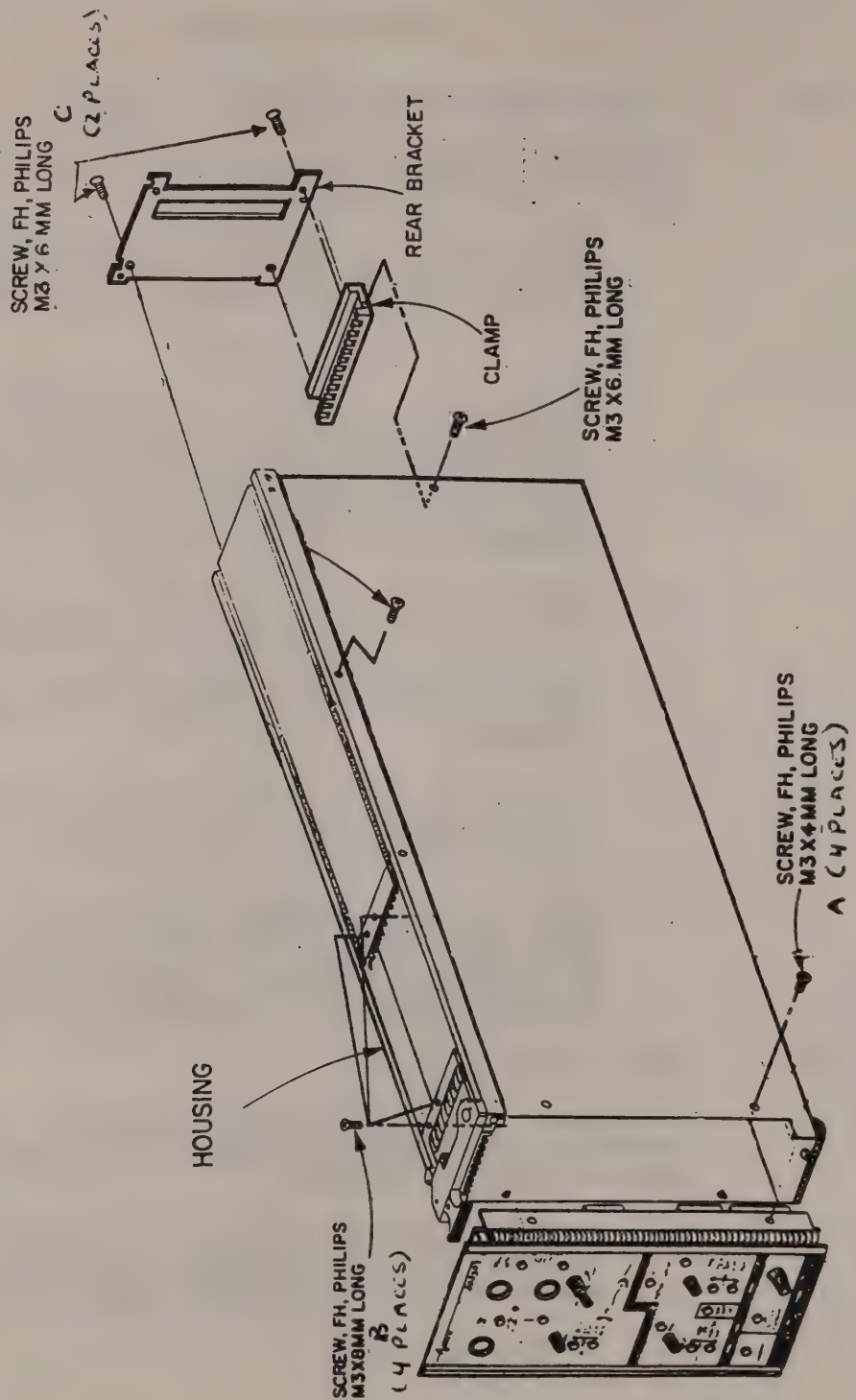


Figure 4-1. Front Panel Assembly and Rail Assembly Removal

4-3 Module Subassembly

The module subassembly (figure 4-2) consists of four board assemblies, the interface (INTF), the memory (MEM or MEMA), the timebase (TMB), and the analog/digital converter (ADC or ADCA). The four board assemblies are mounted on an interconnection assembly (ICON). The module subassembly also includes one subassembly, the amplifier/trigger amplifier (AMP and TAMP), and the external trigger assembly (EXTR). To remove the module subassembly, slide it out of the housing. Removal of the board assemblies, the AMP/TAMP subassembly, and the EXTR are described in the paragraphs that follow.

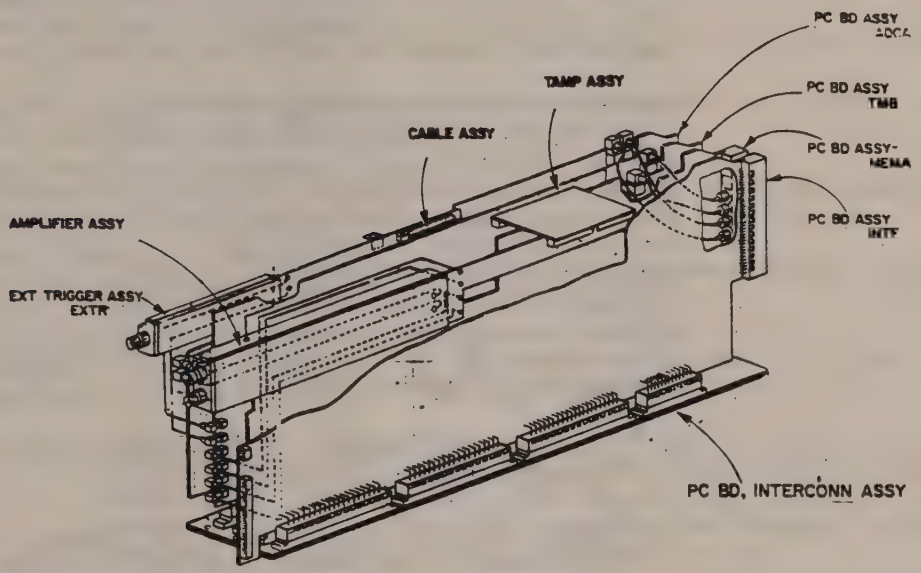


Figure 4-2. Plug-In Module Subassembly

4-3.1 External Trigger Assembly

To remove the EXTR assembly, use the following procedure:

a. Diassemble Module in accordance with procedures in paragraphs 4-1 through 4-3.

b. If EXTR assembly has new-style probe rings, remove tape from side of EXTR assembly and disconnect white wire that connects J1 to INTF assembly (se figure C-1) by pulling gently on yellow insulation sleeving at probe ring end.

c. Not orientation and pull EXTR assembly up to disconnect J3 from P3 on TMB board.

d. Note lead dress and disconnect two cables from connectors J9 and J10 on TMB board, then withdraw disconnected cables from between TMB board and ADC(A) board.

e. Remove disconnected EXTR assembly and place in ESD protective bag.

4-3.2 AMP/TAMP Assembly and ADC(A) Board

The AMP assembly and ADC(A) board must be replaced in pairs because impulse response and bandwidth characteristics vary, making it necessary to adjust the AMP/ADC(A) pairs at the factory for optimum performance. It is necessary to remove both the AMP/TAMP assembly and the ADC(A) board whenever replacement is necessary.

The Plug-In Module uses two types of AMP assemblies. Older Modules have probe rings that are an integral part of the Front Panel Assembly and are connected through the upper pin connector to the INTF board. The probe ring wires are separated automatically when the connector is detached. Newer Modules have probe rings that are an integral part of the BNC connectors on the front and are connected by wires to the INTF board. The configuration of the removed AMP assembly should be noted and specified when ordering a replacement. To remove the AMP/TAMP assembly and ADC(A) board, use the following procedure:

a. Diassemble Module in accordance with procedures in paragraphs 4-1 through 4-3.

b. With Module positioned as shown in figure 4-2, disconnect two short SMB cables from J3 and J4 (see figure). It may be necessary to use edge of flat screwdriver blade to pry REF CLK connector P3 and EXT CLK connector P4 off J3 and J4.

c. If AMP assembly has new-style probe rings, remove tape and pull gently on yellow sleeving to disconnect two white wires fro J1A (CH1) and J5A (CH2).

d. Disconnect two SMB cables (P1 and P2) from J1 and J2 on front of ADC(A) board.

e. Lift EXTR assembly up and out of way, then insert screwdriver in between VME connectors on ICON board and gently pry ADC(A) board up out of connectors J14, J24, J34, and J44 to remove.

f. Disconnect SMB connectors P5, P6, P7, and P8 from J5, J6, J7, and J8 on TMB board. Remove ADC(A) board and place in ESD protective bag.

g. Separate AMP/TAMP assembly from TMB board by using connectors J1 and J2 to lift AMP assembly slightly, then insert one finger between TMB and MEM(A) boards and use gentle, but firm rocking and lifting motion to disconnect TAMP assembly from connectors P1 and P2 on upper edge of TMB board.

h. Push MEM(A) and TMB boards apart gently and remove TAMP assembly from AMP board, being careful to guide wires disconnected in steps d. and f. around twisted pair spools on TMB board. Place removed assemblies in ESD protective bags.

4-3.3 TMB Board

To remove the TMB board, use the following procedure:

a. Diassemble Module in accordance with procedures in paragraphs 4-1 through 4-3.

b. Remove EXTR assembly in accordance with applicable steps of paragraph 4-3.1.

c. Remove AMP/TAMP assembly in accordance with applicable steps of paragraph 4-3.2.

d. Disconnect two short SMB cables (P3 and P4) from J3 and J4 at rear of TMB board (see figure C-1).

e. With Module positioned as shown in figure 4-2, insert screwdriver in between VME connectors on ICON board and gently pry TMB board up and out of connectors J13, J23, J33, and J44 to remove. PLace removed TMB board in ESD protective bag.

4-3.4 Interface Board

Interface boards of two types are used in the Plug-In Module. Old-style probe rings are an integral part of the Front Panel Assebly and are connected through the upper pin connector to the INTF board. The probe ring wires are separated automatically when the connector is detached. New-style probe rings are integral to the BNC connectors on the AMP and EXTR assemblies and INTF boards used in Modules with new-style probe rings are furnished with three white wires for making connections.
The configuration of the removed INTF board should be noted and specified when ordering a replacement.

To remove the INTF board, use the following procedure:

a. Examine INTF board to determine whether replacement should or should not have three white wires for connection to probe rings.

b. Disassemble Module in accordance with applicable steps of paragraphs 4-1 through 4-3.

c. If Module has new-style probe rings, remove tape from AMP and EXTR assemblies, note how wires are connected, and disconnect wires by pulling gently on yellow insulating sleeving at probe ring end.

e. With Module positioned as shown in figure 4-2, insert screwdriver in between VME connectors on ICON board and gently pry INTF board up and out of connectors J11, J21, J31, and J41 to remove. Place removed INTF board in ESD protective bag.

4-3.5 Memory Board

Memory boards of two types are used in the Plug-In Module. The two types are identified as MEM and MEMA. If a Plug-In Module contains a MEM board and it becomes necessary to replace an ADC board, the replacement should be another ADC board or an ADCA board containing 1.7 nSEC variable delay (VARDLY) lines 4 and 5. If a Plug-In MOdule contains a MEMA board, a replacement ADCA board should have 4.9 nSEC VARDLY lines 4 and 5.

To remove a MEM or MEMA board, use the following procedure:

a. Disassemble Module in accordance with applicable steps of paragraphs 4-1 through 4-3.

b. Remove INTF board in accordance with applicable steps of paragraph 4-3.4.

c. Use BNC connectors J1 and J2 to lift front of AMP assembly slightly, then insert one finger between TMB and MEM(A) boards and use gentle, but firm, rocking and lifting motion to disconnect TAMP assembly from connectors P1 and P2 on upper edge of TMB board.

d. Disconnect two SMB cables P3 and P4 from J3 and J4 on rear of TMB board.

e. Disconnect two SMB cables P4 and P5 from J4 and J5 on rear of ADC(A) board.

f. With Module positioned as shown in figure 4-2, insert screwdriver in between VME connectors on ICON board and gently pry MEM(A) board up and out of connectors J12, J22, J32, and J42 to remove. Place removed MEM(A) board in ESD protective bag.

SECTION 5 DISASSEMBLY

5-1 Front Panel Assembly

To disassemble the front panel assembly, use the following procedure:

NOTE

The TIMEBASE and LEVEL knob caps are keyed to reassemble in only one way.

a. Use thin-bladed knife to pry caps (figure 5-1) off TIMEBASE and LEVEL knobs.

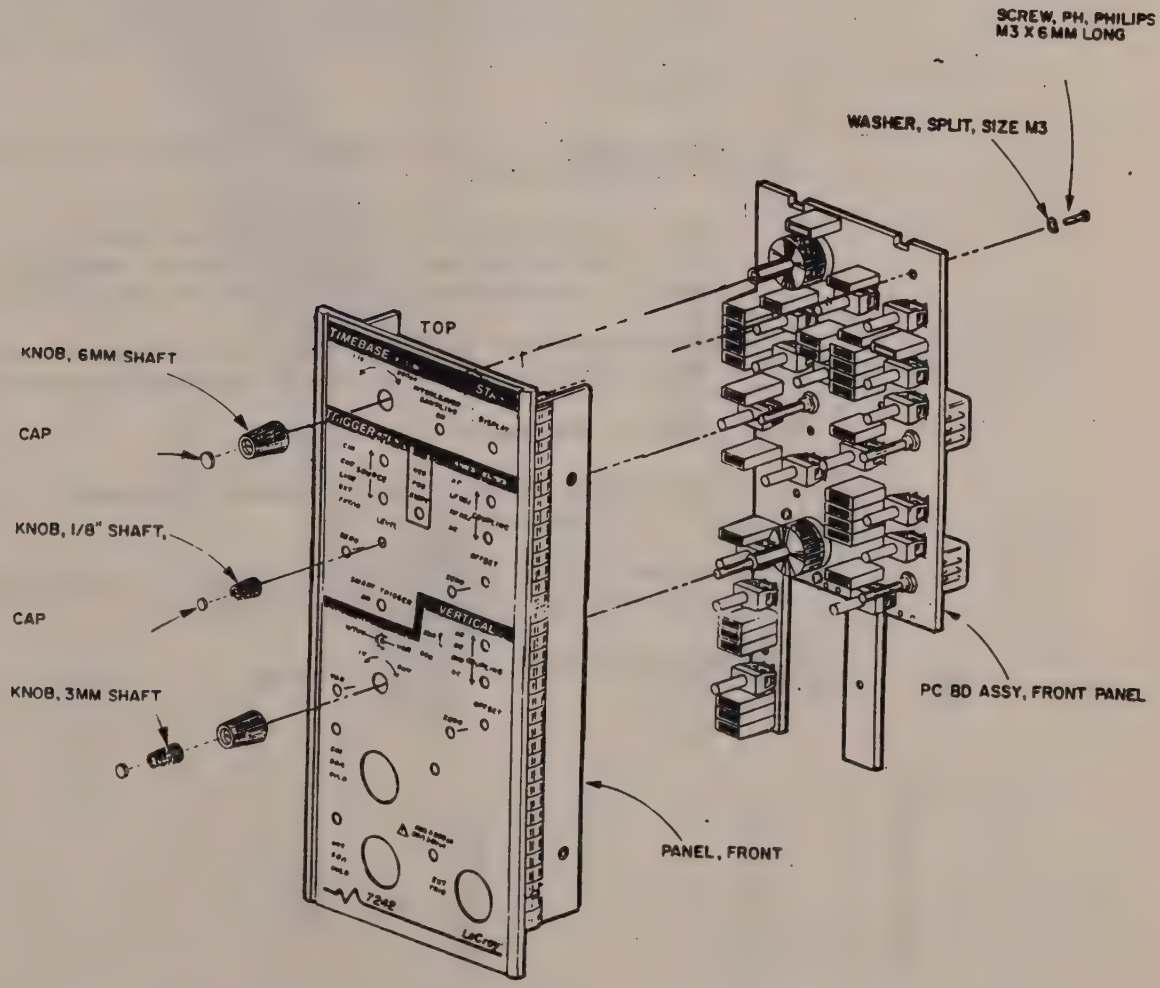


Figure 5-1. Front Panel Assembly Disassembly

b. Use screwdriver to loosen screws inside knobs a half-turn counterclockwise, then remove knobs.

NOTE

The VAR knob cap is keyed to reassemble in only one way.

c. Use thin-bladed knife to pry cap off VAR knob.

d. Use screwdriver to loosen screw inside knob a half-turn counterclockwise, then remove knob.

e. Use nutdriver to loosen nut inside V/DIV knob, then remove knob.

f. From rear of Front Panel, remove 7 Phillips head screws and split washers to remove Front Panel Printed Circuit Board Assembly from front panel.

5-2 Rail Assembly

To disassemble the rail assembly, refer to figure 5-2 and do the following:

a. From top of rail, remove hex nut and split washer to release mylar washer, latch assembly, flat washer, retaining spring, and retaining screw.

b. To remove hex spacer which serves as latch stop, remove Phillips head screw and split washer.

5-3 Rear Bracket Assembly

To disassemble the rear bracket assembly, use the following procedure:

a. Remove 2 flat Phillips head screws (see figure 4-1) that attach clamp to rear bracket.

b. Remove clamp.

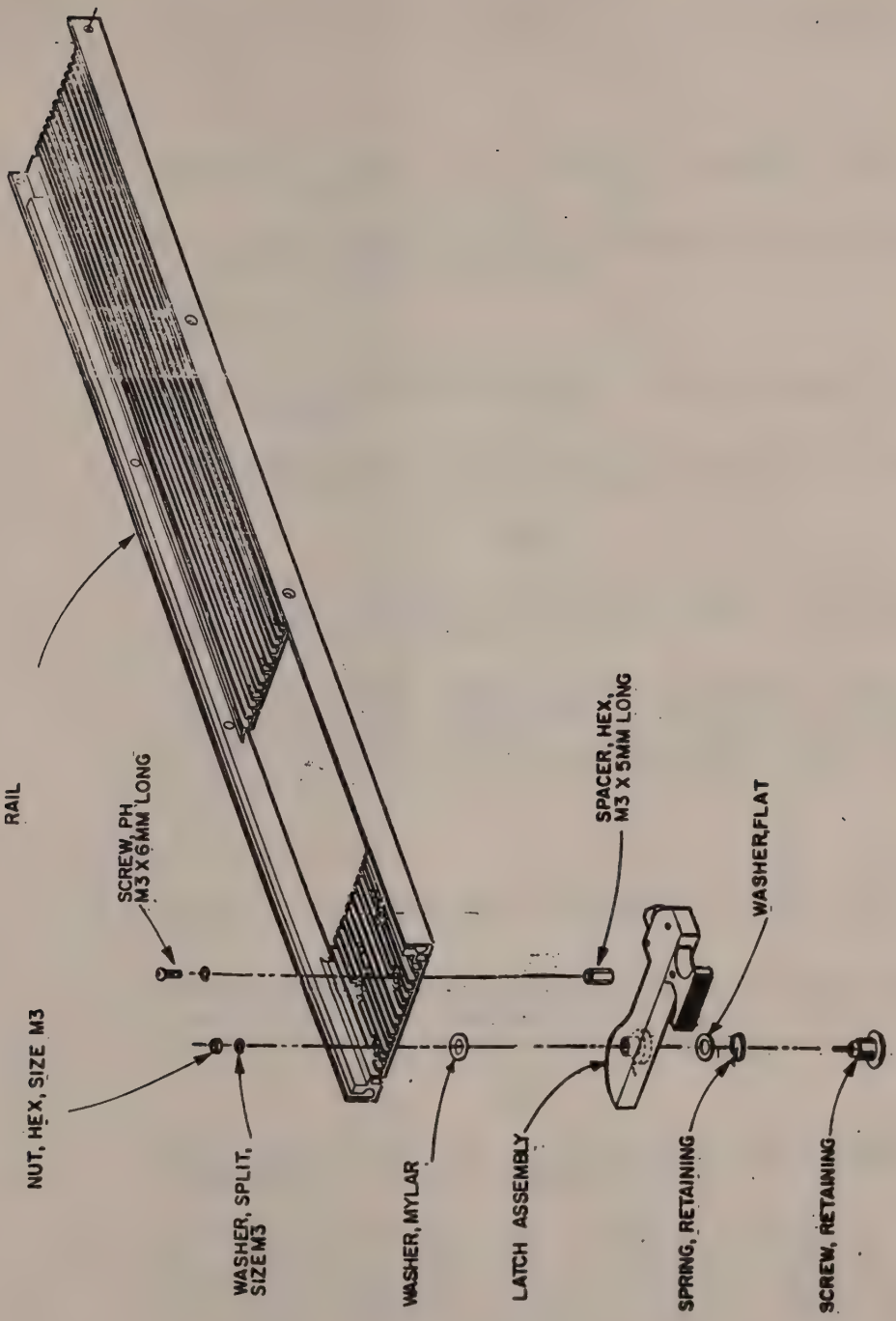


Figure 5-2. Rail Assembly Disassembly

SECTION 6 REASSEMBLY

Reassembly is generally in the reverse order of disassembly. All hardware is tightened during reassembly to the torque limits specified in appendix D.

6-1 Rear Bracket Assembly

To reassemble the rear bracket assembly, use the following procedure:

a. Position clamp as shown in figure 4-1 and reinstall 2 flat Phillips head screws.

6-2 Rail Assembly

To reassemble the rail assembly, refer to figure 5-2 and do the following:

a. Reinstall spacer (latch stop) by reinstalling split washer and Phillips head screw.

NOTE

Be sure to reinstall retaining spring correctly to apply tension to latch.

b. Reinstall flat washer and retaining spring on retaining screw, then insert through latch assembly, reinstall mylar washer, and insert subassembly through bottom of rail and reinstall split washer and hex nut.

6-3 Front Panel Assembly

To reassemble the front panel assembly, use the following procedure:

a. Position front panel printed circuit board assembly (see figure 5-1) behind front panel and reinstall 7 split washers and Phillips head screws.

NOTE

All knobs must be reinstalled with sufficient clearance to prevent binding.

b. At front of Front Panel assembly, reinstall V/DIV knob. Allow sufficient clearance (.020 or about thickness of matchbook cover) between skirt of knob and front panel to prevent binding. Use nutdriver to tighten nut inside V/DIV knob.

c. Reinstall VAR knob. Allow sufficient clearance (approximately .020) between skirt of knob and top of V/DIV knob to prevent binding. Use screwdriver to tighten screw inside V/DIV knob.

d. Align notch in cap with keyway inside VAR knob and snap back into place.

e. Reinstall LEVEL knob. Allow sufficient clearance (approximately .020) between skirt of knob and front panel to prevent binding. Use screwdriver to tighten screw inside V/DIV knob.

f. Align notch in cap with keyway inside LEVEL knob and snap back into place.

g. Reinstall TIMEBASE knob. Allow sufficient clearance (approximately .020) between skirt of knob and front panel to prevent binding. Use screwdriver to tighten screw inside V/DIV knob.

h. Align notch in cap with keyway inside TIMEBASE knob and snap back into place.

SECTION 7 INSTALLATION/REINSTALLATION

The 7242 Plug-In Module is positioned bottom-up for reinstallation of the AMP/TAMP subassembly and the other assemblies, the rear panel, the front panel, and the rail assembly.

Before reinstalling circuit board assemblies in the ICON board, note that fish paper is used extensively to insulate the circuit board assemblies from each other and prevent shorts. Be sure to check each circuit board assembly for missing or damaged fish paper before reinstallation.

7-1 Module Subassembly

The module subassembly consists of the subassembly reinstalled on the INTF board and the circuit boards reinstalled on the ICON assembly.

7-1.1 Memory Board

NOTE

Defective MEM(A) boards should be replaced with the same level board or a higher revision level. Likewise, a defective MEM(A) board should not be replaced with one bearing a lower-level ECO sticker. A MEM board should never be substituted for a MEMA board. Also, a MEM or MEMA board can be installed in a 7242 Plug-In Module containing a ADCA board but a MEMA board cannot be used with an ADC board; an ADCA board is compatible with both a MEM board and a MEMA board.

If an MEM board is to be installed in a 7242 Plug-In Module containing a ADCA board, the variable delay (vardly) lines on the ADCA must be 1.7 nSEC types. If a MEMA board is to be installed in a 7242 Plug-In Module containing an ADCA board, the variable delay (vardly) lines on the ADCA must be 4.9 nSEC types.

To install or reinstall a MEM(A) board, use the following procedure:

a. If MEM(A) board is to be installed/reinstalled, check ADC(A) board to determine compatibility.

b. Dress four cables toward rear of MEM(A) board for later connection to ADC(A) and TMC boards, then install MEM(A) board on ICON assembly, seating firmly in VME connectors J12, J22, J32, and J42.

c. Connect cable P5 and longer P4 cable to J5 and J4 on rear of ADC(A) board.

d. Connect shorter P4 cable and cable P3 to J4 and J3 on rear of TMB board.

e. Install TAMP assembly in accordance with step c. of paragraph 7-1.4.

f. Install INTF board in accordance with applicable steps of paragraph 7-1.2.

7-1.2 Interface Board

Defective INTF boards should be replaced with the same level board or a higher revision level. A defective board should not be replaced with one bearing a lower-level ECO sticker. To install or reinstall an INTF board, use the following procedure:

a. Examine INTF board to determine whether it has three white wires for connection to new-style probe rings.

b. Install INTF board on ICON board, seating firmly in VME connectors J11, J21, J31, and J41.

c. If AMP assembly has new-style probe rings, connect white wires from INTF board to J5A (CH2) and J1A (CH1) by pushing on. If EXTR assembly has new-style probe rings, connect white wire from INTF board to J1E (EXTR) by pushing on. Tape white wires to sides of AMP and EXTR assemblies to prevent interference with Front Panel assembly during reinstallation.

7-1.3 TMB Board

Defective TMB boards should be replaced with the same level board or a higher revision level. A defective board should not be replaced with one bearing a lower-level ECO sticker. To install/reinstall a TMB board, use the following procedure:

a. Install TMB board on ICON assembly, seating firmly in VME connectors J13, J23, J33, and J43.

b. Connect two short SMB cables (P4 and P3) to J4 and J3 at rear of TMB board.

c. Install AMP/TAMP assembly in accordance with applicable steps of paragraph 7-1.4.

d. Install EXTR assembly in accordance with applicable steps of paragraph 7-1.5.

7-1.4 AMP/TAMP Assembly and ADC(A) Board

The AMP assembly and the ADC(A) board must be replaced in pairs. Impulse response and bandwidth characteristics vary and AMP/ADC(A) pairs are carefully adjusted at the factory for optimum performance. Defective AMP and TAMP assemblies should be replaced with the same level assembly or a higher revision level.

Before installing replacements, it should be noted whether the AMP assembly is furnished with old- or new-style probe rings. Old-style probe rings are connected directly to the Front Panel assembly; new-style probe rings are connected to the INTF board.

The type of MEM board used in the Module must be determined to ensure installation of the correct ADC board. If the Module contains a MEM board, an ADC or ADCA board can be used for replacement. If the Module contains a MEMA board, only an ADCA board can be installed.

The ADCA board has four variable delay lines. Variable delay (VARDLY) lines 1 and 3 are adjusted at the factory during board assembly and should not require readjustment in the field. VARDLY line 2 is used to adjust flash ADC and output latch timing. VARDLY line 4 is used to adjust timing of data latching in the ICON assembly and clock pulses which shift data into the MDX802s. Timing varies between Plug-In MOdules and may have to be readjusted in the field.

VARDLY lines 4 and 5 (see figure B-3) must be the proper type for the intended installation. If the MOdule contains a MEM board, delay lines 4 and 5 must be 1.7 nSEC units; if a MEMA board is used, delay lines 4 and 5 must be 4.9 nSEC units.

To install/reinstall an AMP/TAMP assembly and ADC(A) board, use the following procedure:

NOTE

Later production TAMP assemblies include plastic strips which key the connectors and prevent misassembly (see figure B-1). The plastic strips also prevent short circuits between the TAMP assembly and the bottom rail assembly. If a TAMP assembly to be installed is missing the plastic strips, it should be returned to the factory for replacement.

a. Install TAMP assembly on AMP assembly, if not already installed.

b. Position AMP/TAMP assembly for installation and dress six cables between MEM(A) and TMB boards and around twisted pair spools on TMB board.

c. Install AMP/TAMP assembly in such a way that TAMP assembly engages connectors P1 and P2 on TMB board and bridges cutout portion of MEM(A) board.

d. If AMP assembly has new-style probe rings, tape white wires from INTF board to side and connect wires to J5A (CH2) and J1A (CH1) by pushing onto probe rings.

e. Lift EXTR assembly up and out of way and install ADC(A) board in VME connectors J14, J24, J34, and J44 on ICON assembly. Be sure to seat ADC(A) board firmly in connectors.

f. Connect EXT CLK connector P4 from MEM(A) board to J4. Connect REF CLK connector P3 from MEM(A) board to J3.

NOTE

Defective ADC boards should be replaced with the same level board or a higher revision level. Likewise, a defective ADC board should not be replaced with one bearing a lower-level ECO sticker. An ADC should never be substituted for an ADCA. Also, an ADC can be installed in a 7242 Plug-In Module containing a MEM board but cannot be used with a MEMA board; an ADCA is compatible with both a MEM board and a MEMA board.

If an ADCA board is to be installed in a 7242 Plug-In Module containing a MEM board, the variable delay (vardly) lines on the ADCA must be 1.7 nSEC types. If an ADCA board is to be installed in a 7242 Plug-In Module containing a MEMA board, the variable delay (vardly) lines on the ADCA must be 4.9 nSEC types.

On older ADC boards (revision C), the silk screening for CH1 (J1) and CH2 (J2) was reversed on the side with the large HMS403 hybrid circuits. The incorrect marking has been removed from most of these boards. For proper connection, P1 should be installed on the SMB connector closest to the edge of the ADC board and P2 should be installed on the other connector.

g. Connect two SMB cables (P2 and P1) to J2 and J1 on ADC(A) board.

h. Connect P8, P7, P6, and P5 for AMP assembly to SMB connectors J8, J7, J6, and J5 on front of TMB board. Dress cables back between MEM(A) and TMB boards to allow clearance for installation of Front Panel assembly.

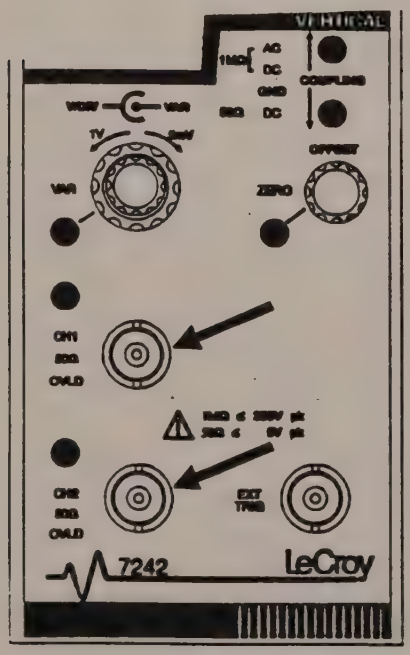
7-2 Rear Bracket Assembly

The rear bracket assembly is reinstalled after the module subassembly has been reinstalled in the housing. To reinstall the rear bracket assembly, use the following procedure:

Refer to figure 4-1 and position rear bracket assembly on rear of housing for reinstallation of attaching hardware. Reinstall 2 flat Phillips head screws.

7-3 Front Panel Assembly

Front panel assemblies of two types have been used on 7242 Plug-in Modules. On some models, the probe ring that surrounds the CH1, CH2, and EXT TRIG BNC connectors (figure 7-1) is an integral part of the front panel assembly. On other models, the probe ring is part of the BNC connectors on the EXTR and AMP assemblies. The front panel assembly must be reinstalled carefully on the latter models to avoid damage to the thin nylon insulating rings that surround the BNC connectors. To install or reinstall a front panel, use the following procedure:



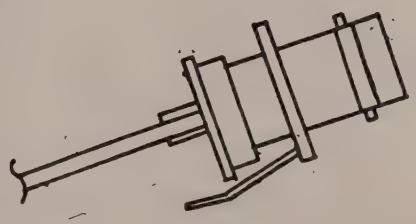
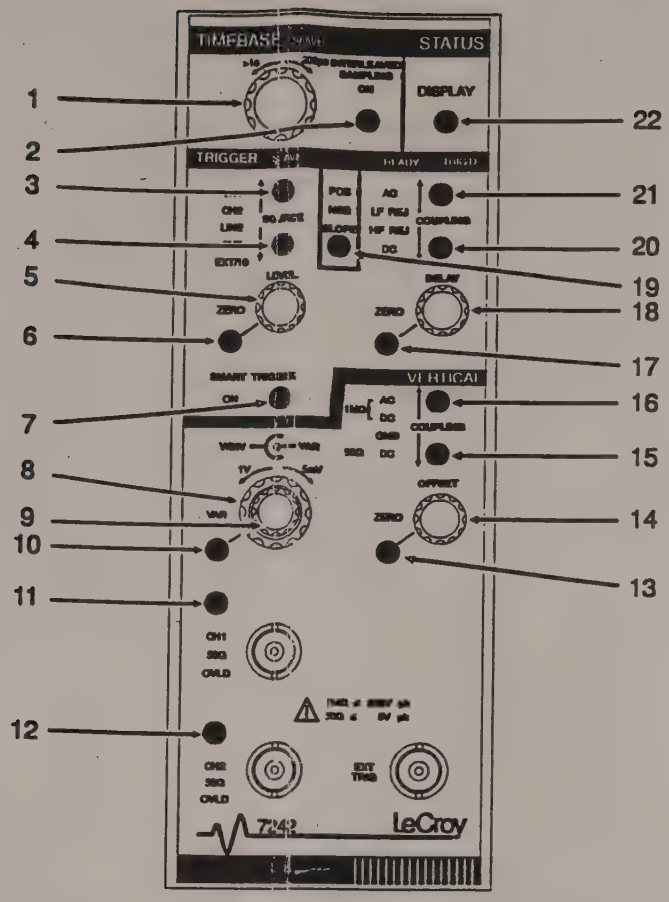


Figure 7-1. Probe Rings

APPENDIX A

FRONT PANEL



1	**TIMEBASE** knob
2	**INTERLEAVED SAMPLING** key
3	Upper Trigger **SOURCE** key
4	Lower Trigger **SOURCE** key.
5	Trigger **LEVEL** knob.
6	Trigger Level **ZERO** key
7	**SMART TRIGGER** key.
8	**V/DIV** knob.
9	**VAR** knob.
10	**VAR** key.
11	**CH1** key
12	**CH 2** key
13	Vertical Offset **ZERO** key.
14	Vertical **OFFSET** knob.
15	Lower Vertical **COUPLING** key
16	Upper Vertical **COUPLING** key.
17	Trigger Delay **ZERO** key
18	Trigger **DELAY** knob.
19	Trigger **SLOPE** key
20	Lower Trigger **COUPLING** key
21	Upper Trigger **COUPLING** key.
22	Plug-in Status **DISPLAY** key

Figure A-1. Front Panel

APPENDIX B

ASSEMBLIES AND BOARDS

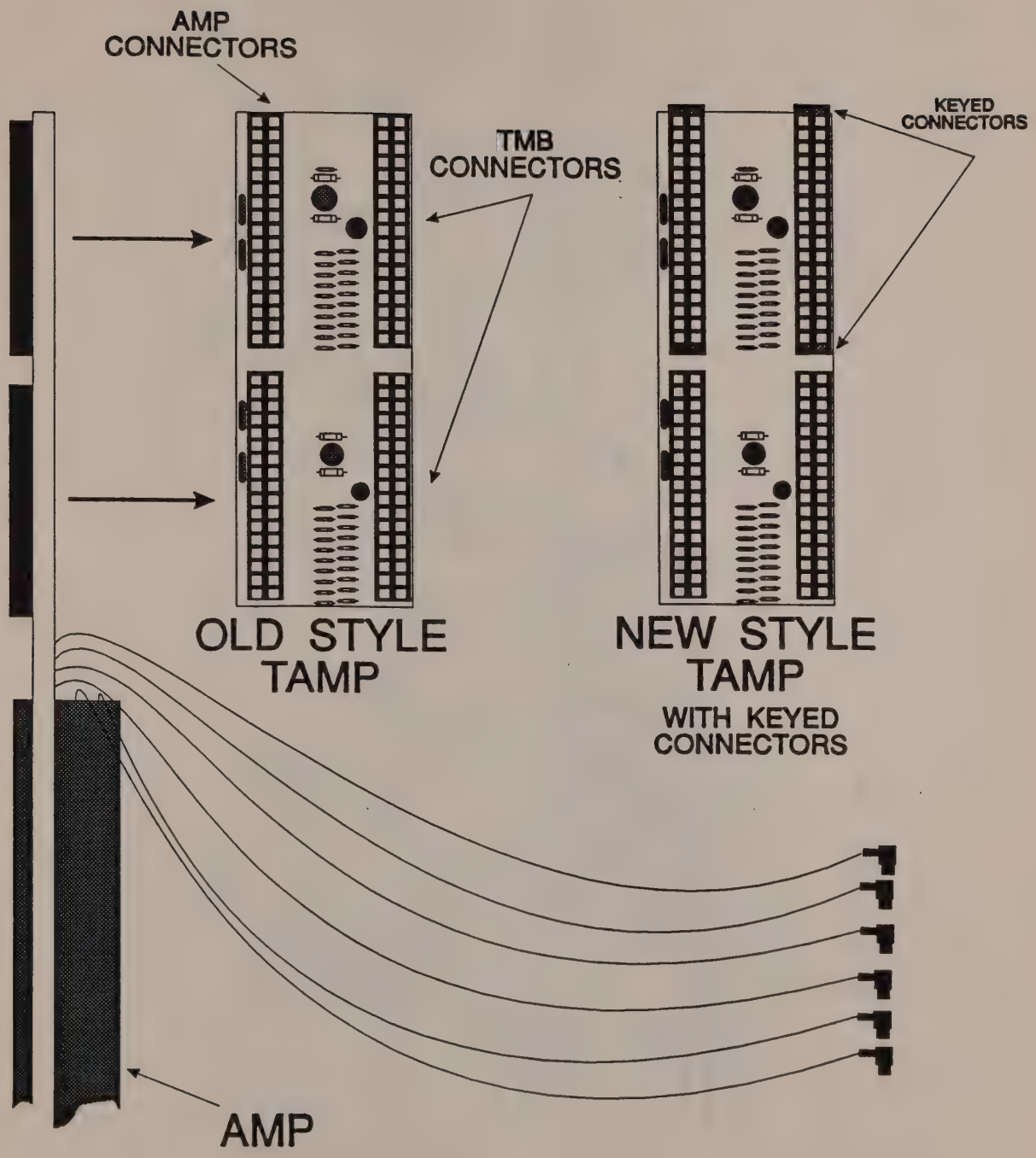


Figure B-1. AMP/TAMP Assembly

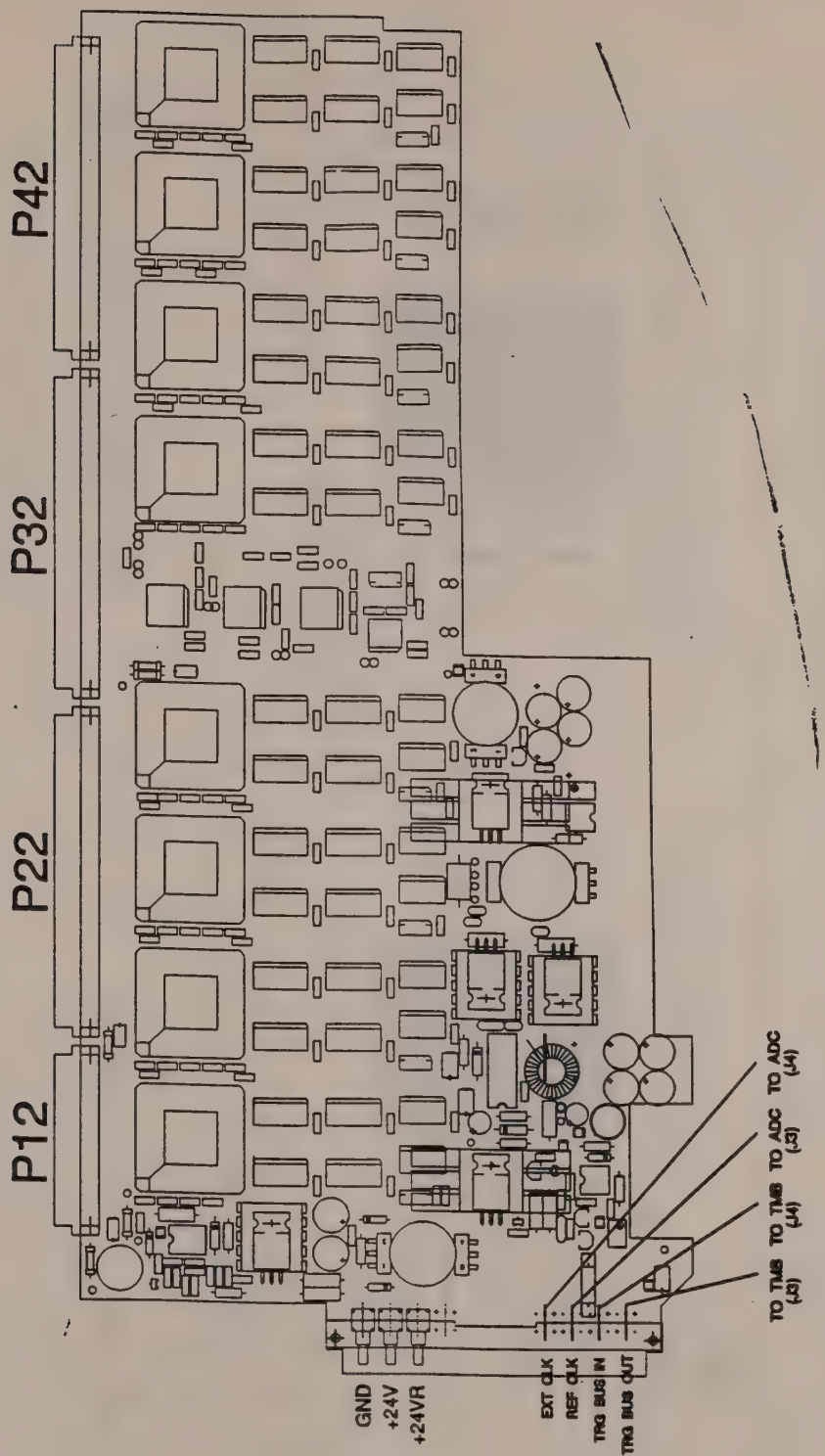


Figure B-2. MEM Board

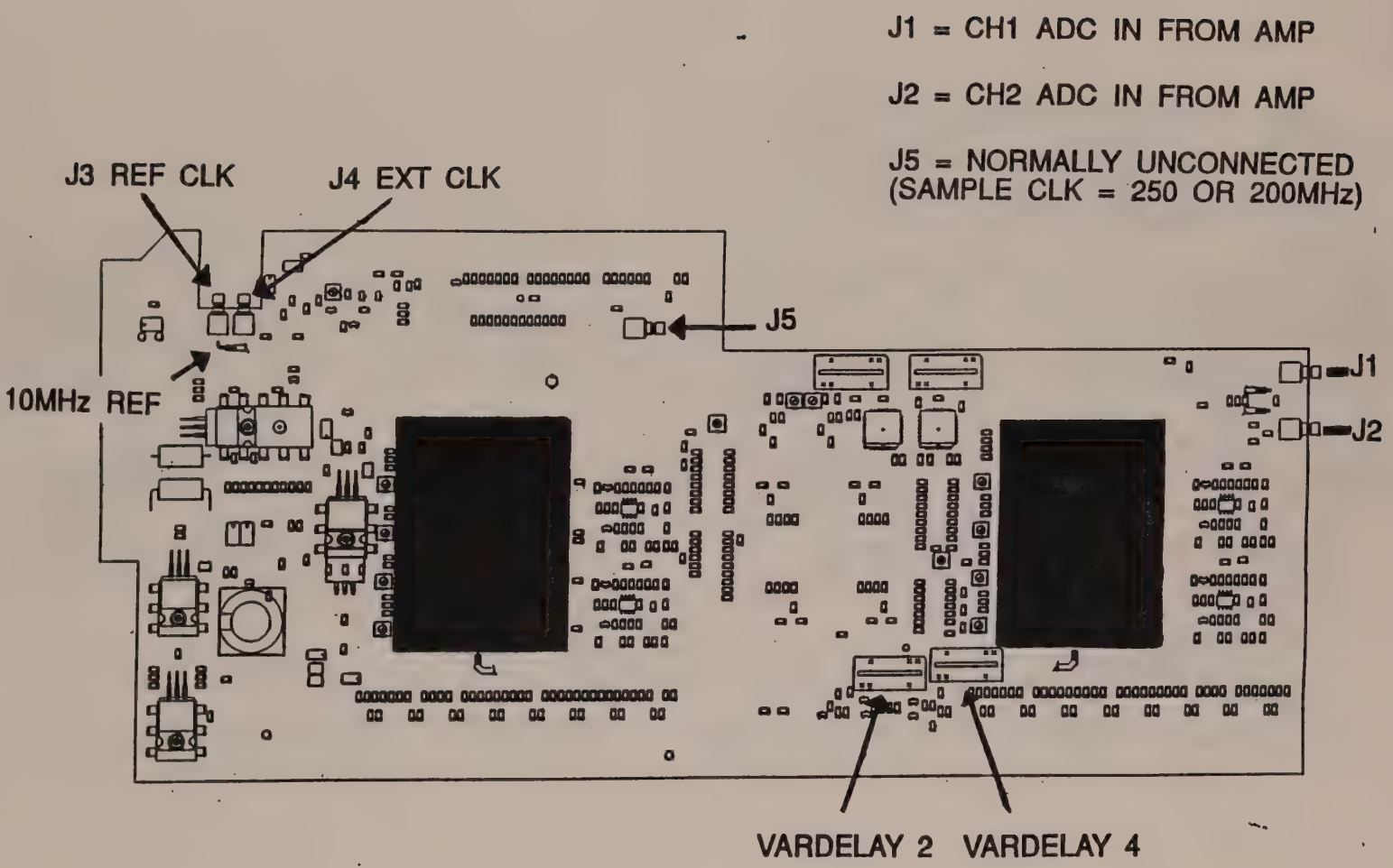


Figure B-3. ADC(A) Board (Sheet 1 of 2)

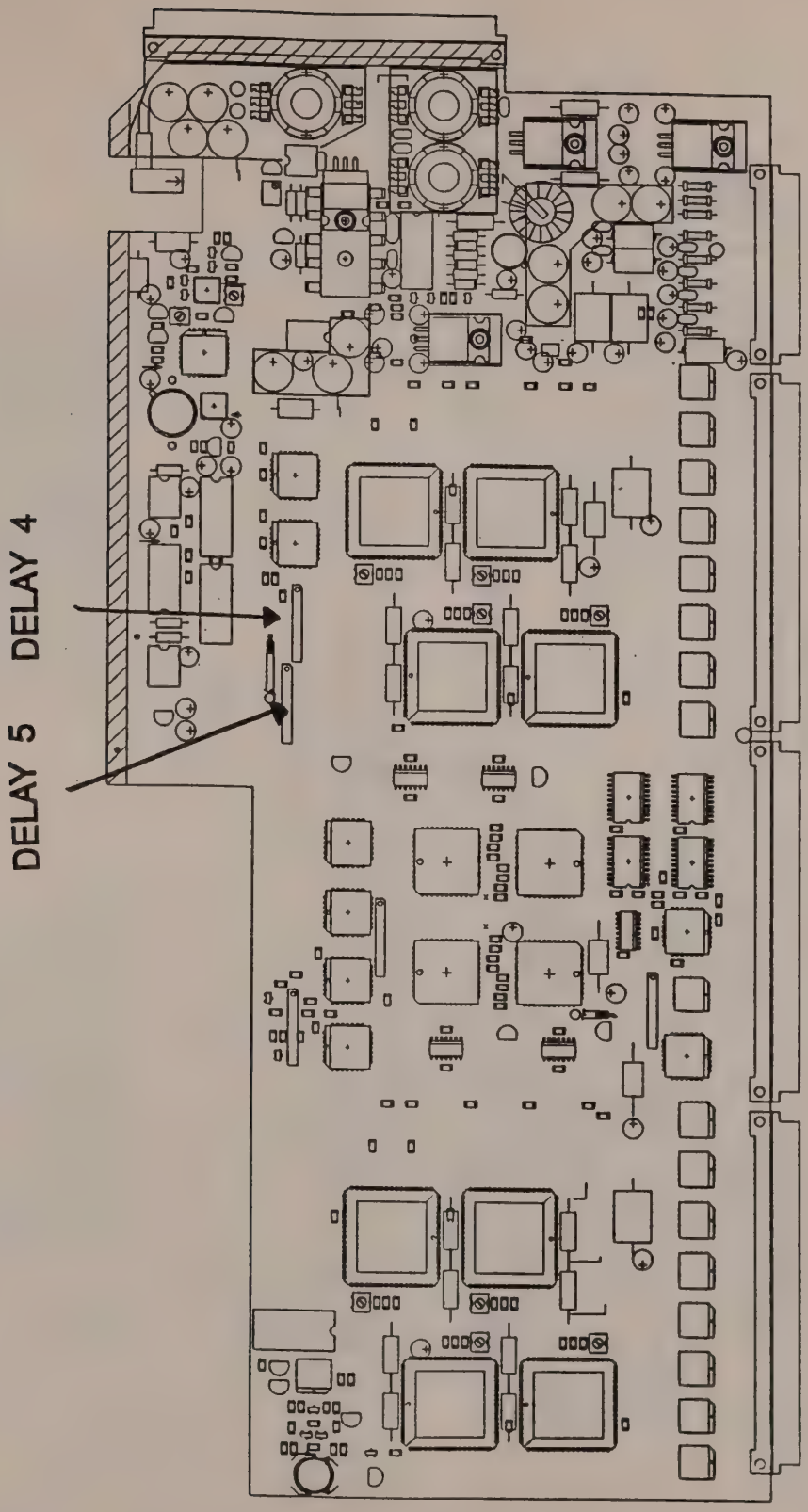


Figure B-3. ADC(A) Board (Sheet 2 of 2)

P1 = CH1 CONTROL TO AMP
P2 = CH2 CONTROL TO AMP
P3 = CONTROL TO EXTRG
J3 = TRIG BUS FROM MEM C
J4 = TRIG BUS FROM MEM C
J5 = CH1 TRIGGER FROM AMP
J6 = CH1 TRIGGER FROM AMP
J7 = CH2 TRIGGER FROM AMP

J8 = CH2 TRIGGER FROM AMP
J9 = EXT TRIGGER FROM EXTR
J10 = EXT TRIGGER FROM EXTR
P13 = VME BUS CONNECTOR
P23 = VME BUS CONNECTOR
P33 = VME BUS CONNECTOR
P43 = VME BUS CONNECTOR

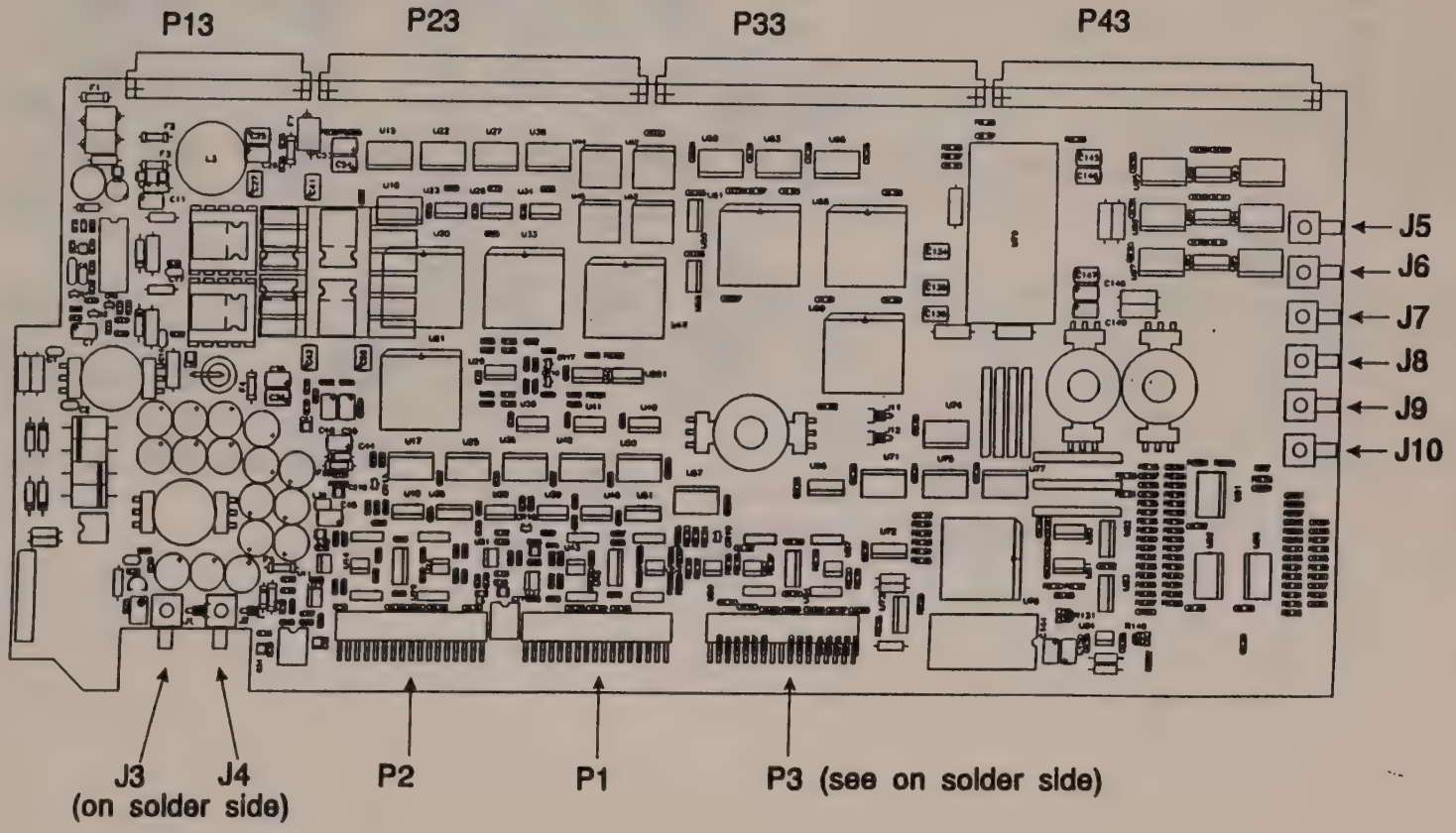


Figure B-5. TMB Board (Sheet 1 of 2)

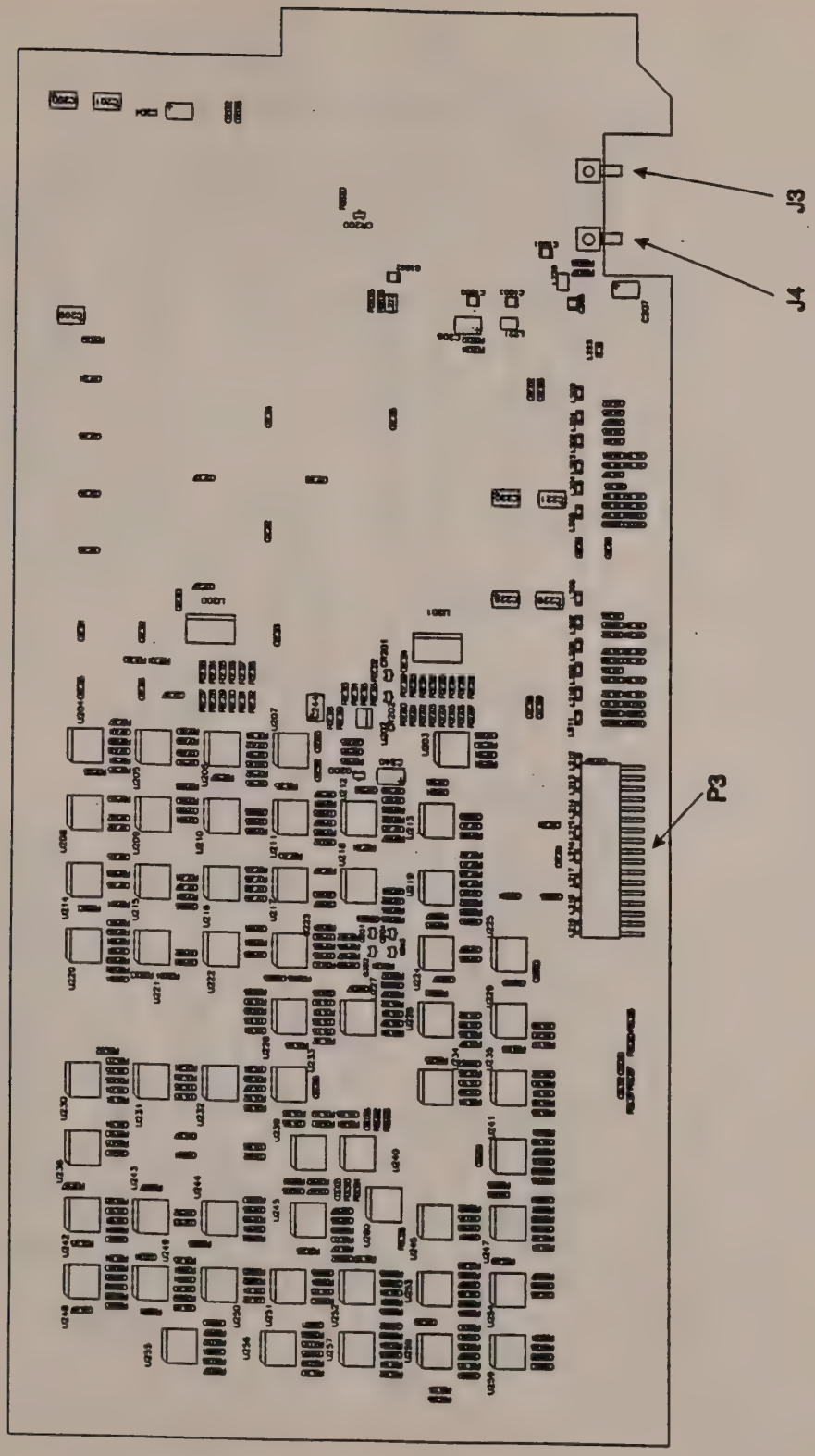


Figure B-5. TMB Board (Sheet 2 of 2)

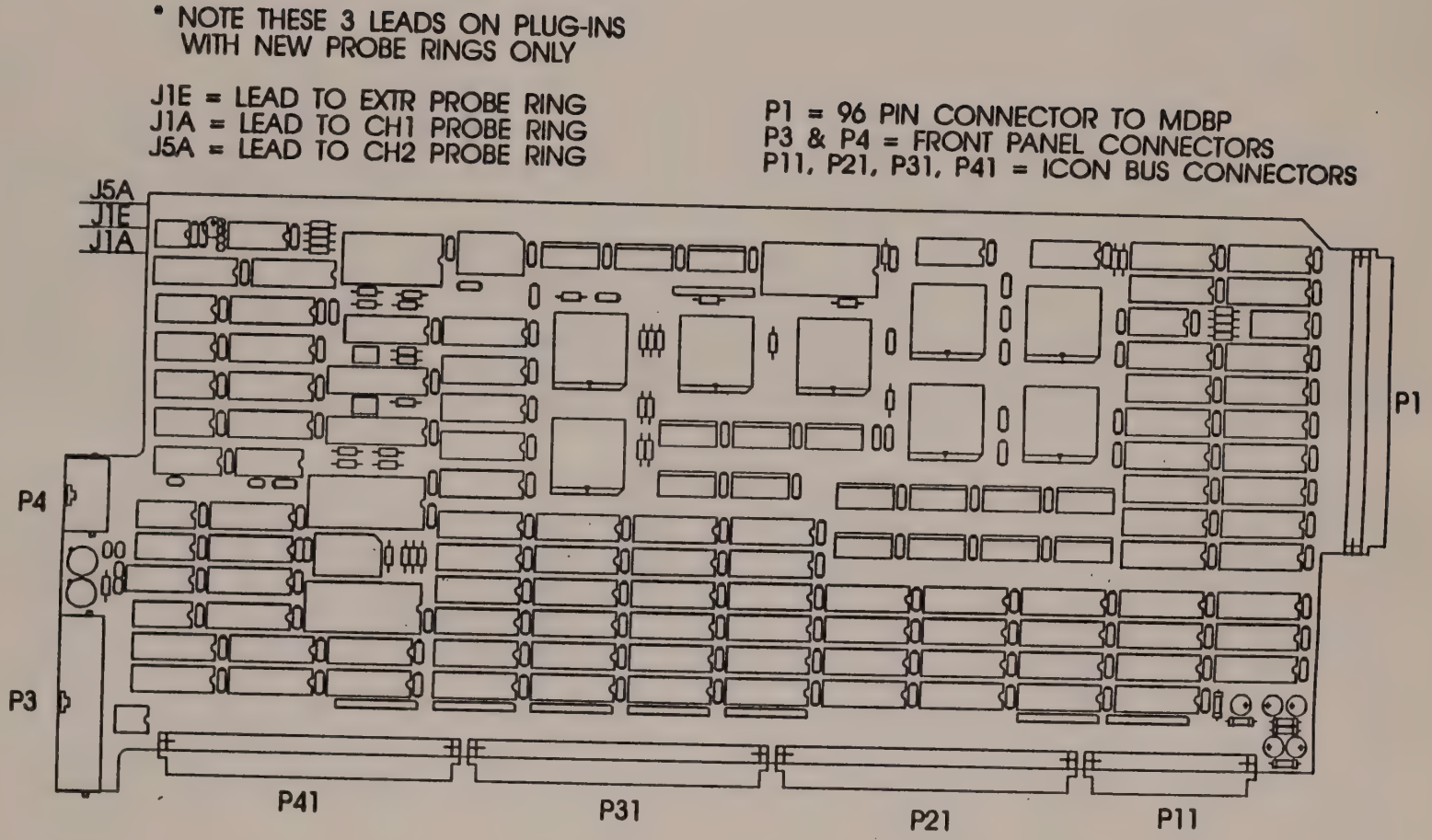


Figure B-6. INTF Board

APPENDIX C

WIRING DIAGRAM

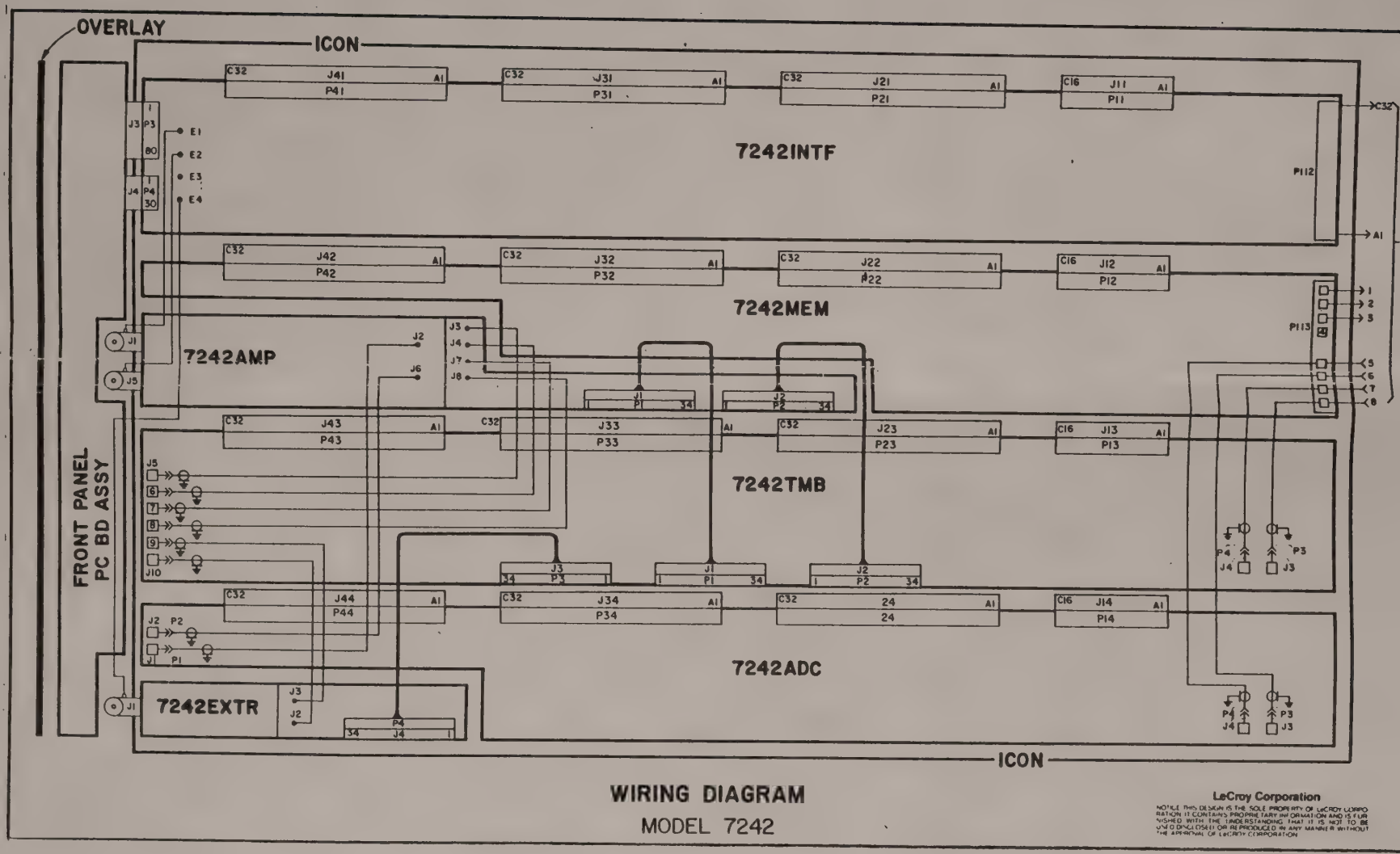


Figure C-1. Wiring Diagram

APPENDIX D

TORQUE VALUES

TORQUE SPECIFICATIONS

7200MAIN ASSEMBLY

3 INCH LB	BOTTOM REAR FEET TO BOTTOM COVER (M3)
8 INCH LB	HOLD DOWN BARS TO WIRE CAGE (M3) DISPLAY BD ASSY TO SIDE PANEL (M3) TILT STAND TO BOTTOM COVER (M3) DISK DRIVE TO DISKMOUNT (6-32)
10 INCH LB	TOP COVER TO SIDE PANELS (M3) BOTTOM COVER TO SIDE PANELS (M3) BOTTOM COVER TO WIRE CAGE (M3)
11 INCH LB	FRONT PANEL ASSY TO SIDE PANELS (M4) REAR PANEL ASSY TO SIDE PANELS (M4)

7200CAGE ASSEMBLY

6 INCH LB	PLASTIC RAILS TO WIRE CAGE (M2.5) SHIELD BRACKET TO MFBP BD ASSY (M3) CARD GUIDE TO MFBP BD ASSY (M3)
8 INCH LB	LOCATING PINS TO WIRE CAGE (M3) FLOPPY DRIVE TO WIRE CAGE (M3) MDBP BD ASSY TO WIRE CAGE (M3) MFBP BD ASSY TO WIRE CAGE (M3)
11 INCH LB	SIDE PANELS TO WIRE CAGE (M4) CRT ASSY TO WIRE CAGE (M4) HANDLE TO SIDE PANEL (#6 & #10 HEX NUT)

7200REAR ASSEMBLY

3 INCH LB	REAR RUBBER FEET TO REAR CASTING (M3)
8 INCH LB	FANS TO REAR CASTING (M3) FAN HOOD TO REAR CASTING (M3) VICOR MODULES TO REAR CASTING (M3) PWR BD TO REAR CASTIMG (M3) PWR SHLD ASSY TO REAR CASTING (M3) BPIFA TO REAR CASTING (M3) SMA TO REAR CASTING (M3) CHASSIS GND CABLE TO REAR CASTING (M4 HEX NUT)

TORQUE SPECIFICATIONS

7200BPIFA ASSY

7 INCH LB	RS232 CABLE ASSY TO BPIFA PANEL PRINTER CABLE ASSY TO BPIFA PANEL GPIB CABLE ASSY TO BPIFA PANEL AC RECEPTACLE TO BPIFA PANEL

7200FRNT ASSY

7 INCH LB	FPCB ASSY TO FRONT CASTING (M3)
2 INCH LB	KNOBS TO SHAFTS

NOTE: M2 SCREWS (2 PLACES) TO MOUNT FPCB TO FRONT CASTING MUST BE TORQUED JUST ENOUGH NOT TO DEFLECT PC BD.

7200 PC BD ASSY'S

7 INCH LB	VME CONNECTORS TO MDBP ASSY (M2.5) LOCATING PINS TO MDBP ASSY (M3)
	LOCATING PINS TO MFBP ASSY (M3)
	FPCBB ASSY TO FPCB ASSY (M3)
	H-V SHIELDS TO DSPL BD (M3) DSPL HEATSINK TO DSPL BD (M3)

7200SHLD ASSY

5 INCH LB	SET-SCREWS OF CONNECTORS: J104, J134 & J135
8 INCH LB	#4 MTG HDWR FOR CONNECTOR J34

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